480Z
SERVICE MANUAL

October 1984

380Z AND 480Z SYSTEMS

SERVICE MANUAL

PN 13821

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SECTION 1

THE KEYBOARD

(Circuit ref. : Alphameric Drawing no. 146-1710)

There are 64 keys, each generating a distinct 8-bit code (not ASCII) whenever it is pressed or released, accompanied by a strobe pulse. In fact, only 6 bits are used, with bit 8 indicating key position (0 = down, 1 = up). The keyboard consists, electrically, of an 8 x 8 matrix which is scanned to check key status (up or down). This scanning is accomplished by 3 IC's:

1. IC 8 is a 12-stage binary counter clocked by oscillator IC5b/IC6a at about 500 kHz. The clock is divided by 8 (Q0, Q1, and Q2 are not used) and then again by 8 (Q3, Q4 and Q5 are used for strobe functions) to give a 6-bit key address count which is placed on the data bus. This forms part of the data byte sent to the processor and is accompanied (if a key has changed state) by a strobe pulse and DEPRESSION signal.

2. IC 7 is a decoder which takes the three most significant bits of the key address and enables the appropriate row of the matrix, provided that the 'D' input is low. As 'D' is connected to the 500 kHz clock, each row in turn outputs a 500 kHz signal.

3. IC 1 is an analogue-type multiplexer: each of the inputs 0 to 7 is at high impedance, except for the one selected (by pins 9, 10, 11) which is connected via a few hundred ohms resistance to the Z output. Input selection comes from the three least significant bits of the key address, and so this forms the rest of the scanning operation.

   Each key provides a capacitance coupling between its row and column, and, when pressed, couples the 500 kHz clock to the Z output of IC 1 at the appropriate point in the scanning cycle. The function of the circuitry around IC 2 is to detect whether or not the selected key is pressed. It operates as follows:

   (N.B. IC 2 transistors will be referred to as TR1 to TR5 from left to right).

   - Selected key not pressed

     R9 and D1/D2 provide a 1.5V reference for the base of TR2 and for each of the matrix columns via 4k7 resistors. The output of IC 1 is at high impedance and so a small DC current flows into TR1 (via L1) and TR2 bases. As TR2 collector is stable, no current flows through C3, TR3 has no base current and is turned off, and any small residual charge on C4 is insufficient to drive TR5 base. Consequently, TR5 collector is high.

- Selected key pressed

  There is now a 500 kHz signal from IC 1 (referenced to D2+) which is amplified by the resonant circuit L1/C2, causing the current through TR1 to oscillate. The current through TR2 oscillates in anti-phase and an amplified 500 kHz signal appears at the collector. C1 prevents the oscillation from affecting the base of TR2. During negative half-cycles, C3 pulls the emitter of TR3 lower than its base (held by C4) and it then starts to conduct, charging C3. During positive half-cycles the charge on C3 flows through D3 (TR3 now turned off) to carge C4 and provide a base current for TR5.
  Thus TR5 collector is low.

Once a key address has been set in IC 8, some time elapses to allow a charge to build up on C4, if the key is pressed (see timing diagram, figure 1); the state of TR5 collector is then clocked into IC 3a. The output of this represents the state of the key and forms part of the data byte sent to the processor (as DEPRESSION). At the start of each key address cycle, the Q output of IC 3b turns on TR4 for a short period to ensure that no residual charge remains on C4 from the previous cycle.

As the keyboard must only generate strobe pulses when a key changes state, some sort of memory is required; this is IC 4, a 64-bit shift register. At the start of each address cycle the state of the previous key (latched in IC 3a) is clocked into IC 4, an action which continues as the keyboard is scanned. As IC 4 is clocked, the state of the currently addressed key during the last scan appears at the output and is compared with its present state by IC 5a. If a change has taken place, a strobe is generated near the end of the cycle by IC 6b and IC 6d.

Holding RESET 'low' has the effect of clearing the shift register to all 1's, and not allowing any key depressions to enter IC 3a.

Keyboard scanning is inhibited (as are strobe pulses) by taking the READY line low (stopping 500 kHz oscillator); this happens automatically when the 480Z receives a strobe, and is returned to normal when the CPU reads the keyboard data.

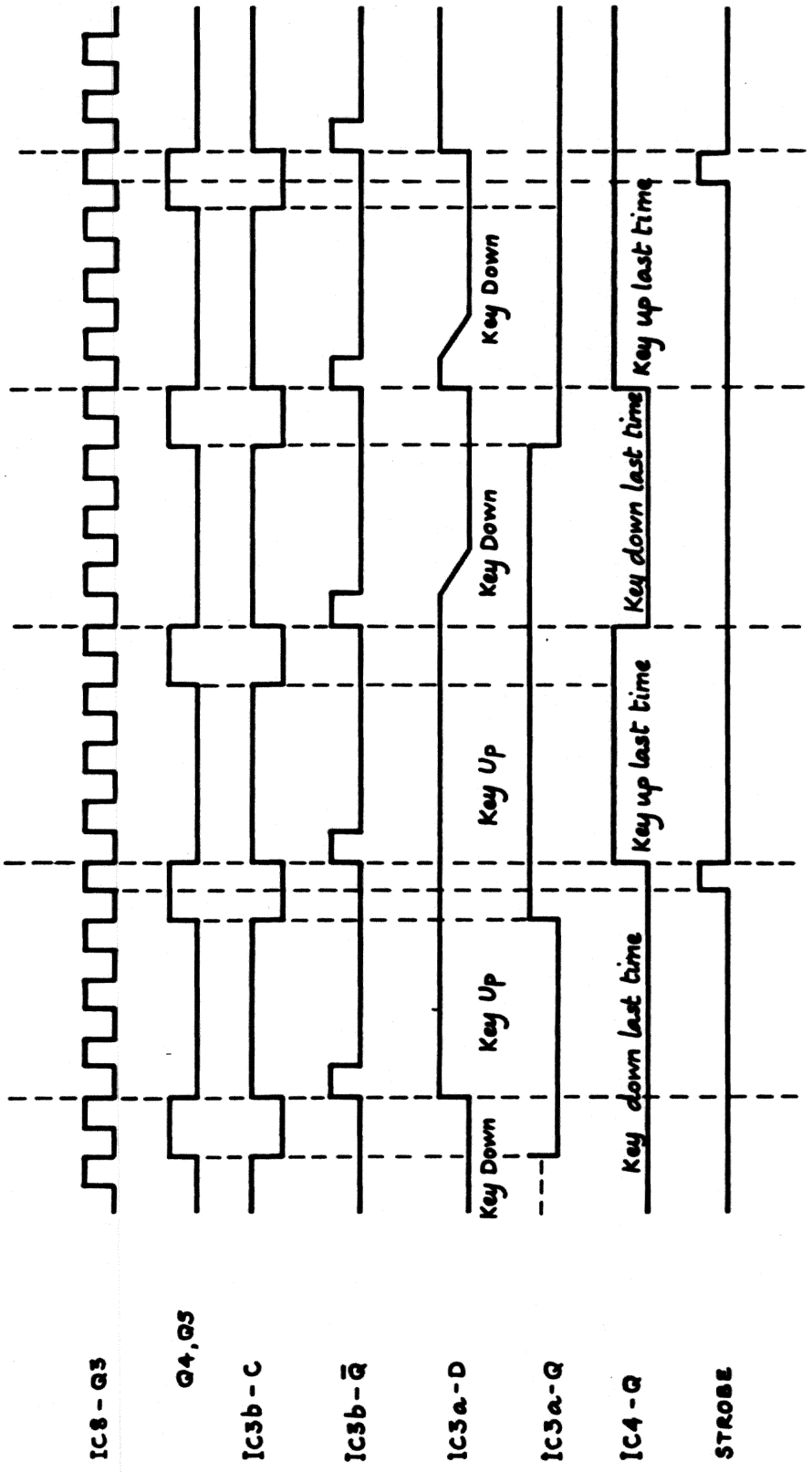

Figure 1.1 Keyboard Timing

SECTION 2

MAIN PCB

(Circuit ref. : D10829, Sheets 1 to 6)

SHEET 1

The Z80A microprocessor is the heart of the system. It is clocked at 4MHz from the oscillator (sheet 4), and all signals directly connected to this are prefixed by Z (e.g. ZWAIT).

To save using high-speed memories, one 'wait' state is inserted in each memory cycle by GT. One 'wait' state is also inserted into each video access (to be described later) to make this transparent to the user. Figure 2.1 shows the relationship between the various derivations of the 4MHz clock, and the timing of GT.

All address lines go through buffers which are permanently enabled, as do some control signals. During I/O cycles, lines A0 to A6 contain the port address, and the most significant lines A2 to A6 are decoded by JS (the port mapping PROM) when enabled by IORQ.

In this system, the Z80 operates in interrupt mode 2, and no port is enabled during interrupt acknowledge cycles as the interrupting device is automatically enabled by the combination of ZMI and ZIORQ being active. Figure 2.2 shows the operation of JS. If the group of system ports is selected (PORTEN low) the address is further decoded (A0 - A2) by CU and DR giving 5 read and 5 write ports, which are used for control and status information, etc. (as shown on sheet 5).

The 'Z' data bus is used directly by ROM and RAM, and is buffered to give a 'T' data bus when TDBUSEN is active. This is used mainly by I/O ports and is further buffered by DQ (write) and CQ (read) for use by VDU circuitry.

When NMIEN goes active (by writing to system port 0) an NMI will be generated during the eighth successive instruction. This is used by the ROS monitor for single-stepping through programs.

The power up circuitry (C23, GW etc) holds the CL line of GU low, and so holds RESET low, until the power rails have stabilised. Memory contents can be corrupted during reset in two ways:

1. While RESET is active no refreshing takes place.

2. If RESET goes active during T3 of an M1 cycle, a short MREQ pulse can be generated which may destroy data.

   Thus, in order to preserve memory contents, the RESET button signal is gated with R3 (part of the row counter in video circuit which happens to be a convenient frequency) and synchronized with M1. This results in RESET being active for 128us, and inactive for 512us, while the button is pressed, allowing sufficient time to

refresh the whole of memory.

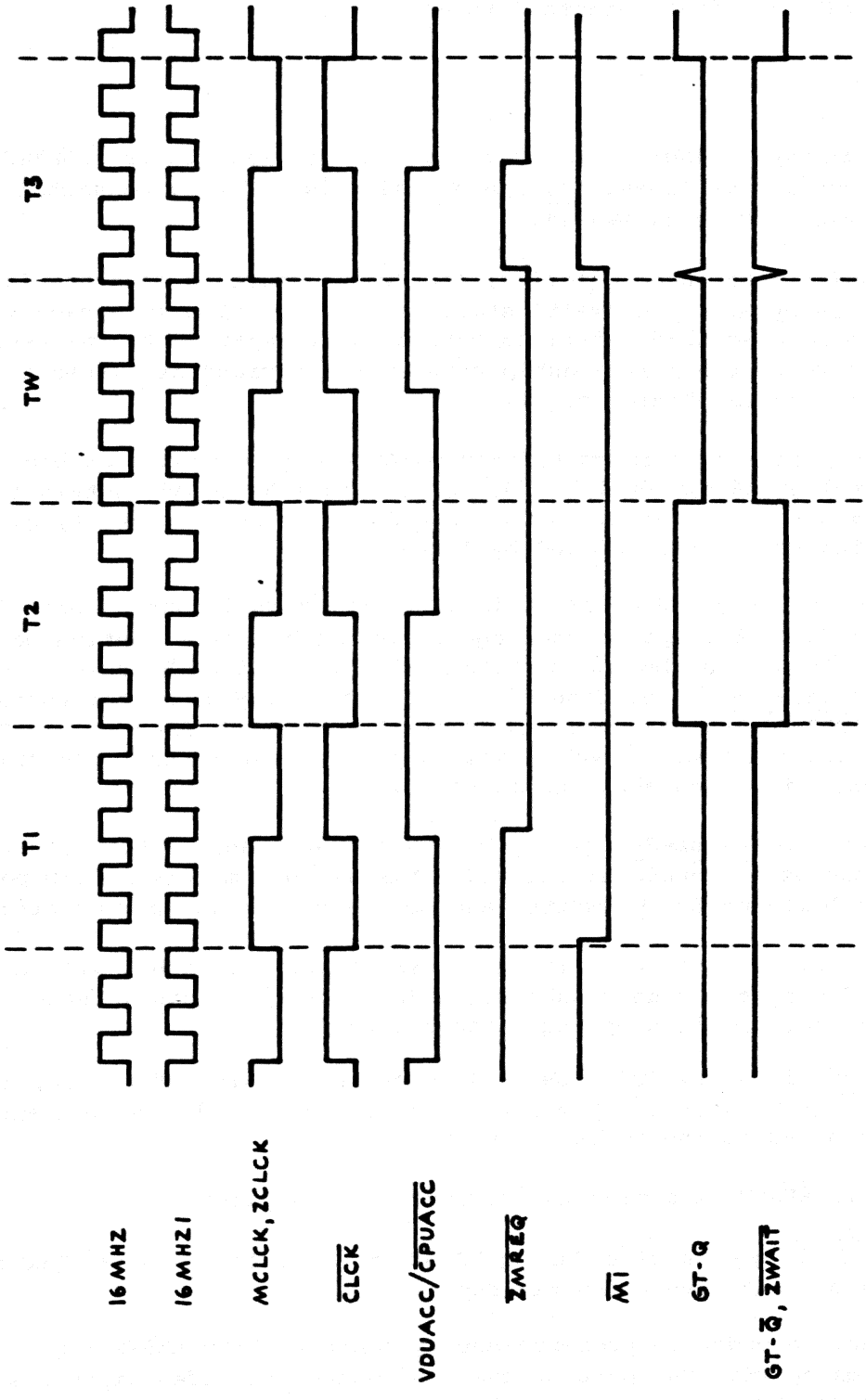

Figure 2.1 Basic M1 Cycle and Clocks

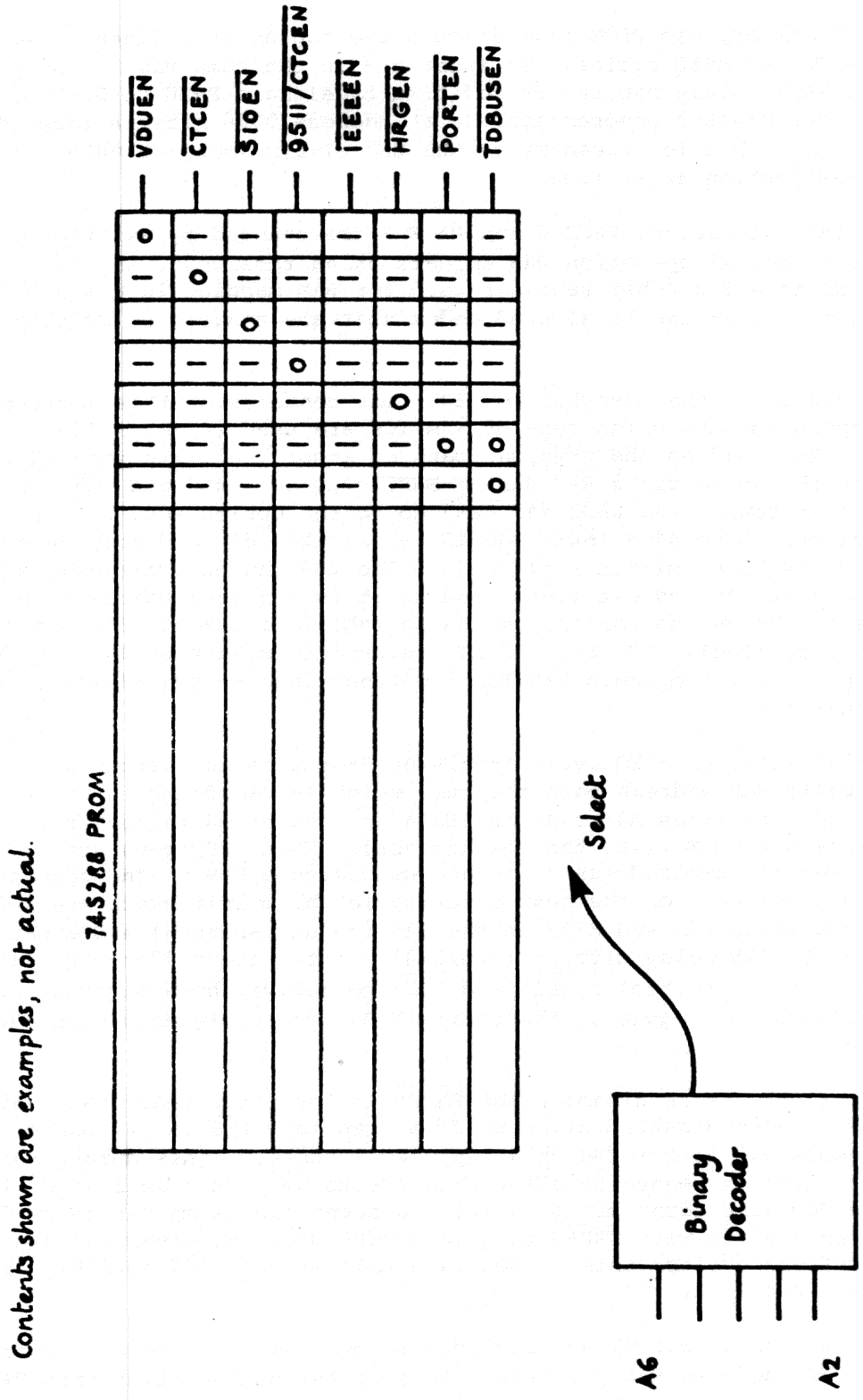

Figure 2.2 Port Mapping

SHEET 2

JV is the memory map PROM that decodes the top address lines to enable RAM or ROM during MREQ cycles. It functions in the same way as the port mapping PROM. This map can be modified by signals PAGE 0, PAGE 1, and ZRD so that the monitor program appears at address 0000 after a reset during memory read; this is necessary as the Z80 always looks at 0000 for its first instruction after reset.

During initialization, PAGE 0 and PAGE 1 are changed by writing to port 1, so that in normal operation RAM appears at address 0000, as required by CP/M. ER is a 4 x 4-bit register used for RAM mapping in a similar way to JV except that it can be altered under software control by writing to port 0.

Figure 2.3 shows the operation of ER. The contents of this register will vary depending upon which type of RAM ICs are used (4116 or 4164). Lines MA16 and MA17 define the physical bank of memory, and are decoded by JT to generate the appropriate RAS during MREQ cycles. RAS0 and RAS1 go to RAM on the main board, and RAS2 and RAS3 go to the option PCB. Lines MA14 and MA15 are used when 4164 (64K) RAM ICs are installed, and they select the required 16K block within a 64K bank. The Z80 can only directly address 64K of memory (16 address lines) and so it is the responsibility of the program to change the contents of ER to make full use of 256K memory (if this is installed). MR, KR, and HT are used to multiplex 14 address lines into 7 pins on the dynamic RAM ICs (16 lines into 8+ for 4164's), and HT also generates CAS.

Figure 2.4 shows an MREQ cycle involving RAM; this is started when the Z80 puts a valid RAM address onto the bus, which is decoded by JV to give RAMEN. Address lines A0 to A6 and MA14 are connected through the multiplexers to RAM (i.e. the row address). When MREQ goes active, JT decodes the top two address lines and generates a RAS on the appropriate bank. At the start of the next clock cycle the multiplexers are switched to connect A7 to A13 and MA15 to the RAM (column address) and RAMEN is connected to CAS delay circuit (R44/C20). After about 40us (to allow address lines to settle) a CAS0 and CAS1 go active; both signals are identical and CAS 1 goes to the option PCB. The cycle ends when MREQ goes inactive.

During refresh, JV is disabled and RAMEN is not generated; this inhibits CAS. ER is also disabled allowing JT to generate RAS on all banks of RAM simultaneously. As the Z80 only supplies 7 address lines during refresh, one extra line is needed to allow 4164 ICs to be used. This is derived from the VDU line count using L1 which changes approximately every 1.5 ms. L1 is synchronized with ZRFSH to give 8RFSHB which is gated through HT during refresh cycles; this allows each half of the 4164's to be refreshed within the 2ms limit.

The two latches GT and GV are included to overcome a timing restriction of dynamic RAM known as RAS precharge: this is the minimum time that RAS must be inactive between memory accesses. This is at its limit between M1 and refresh cycles where ZMREQ goes inactive slightly after the rising edge of

T3 clock, and active again on falling edge. GV terminates RAS (by MRINH to JT) and CAS (by disabling MREQ1) on the rising edge of T3 clock, so overcoming any delay in ZMREQ going high.

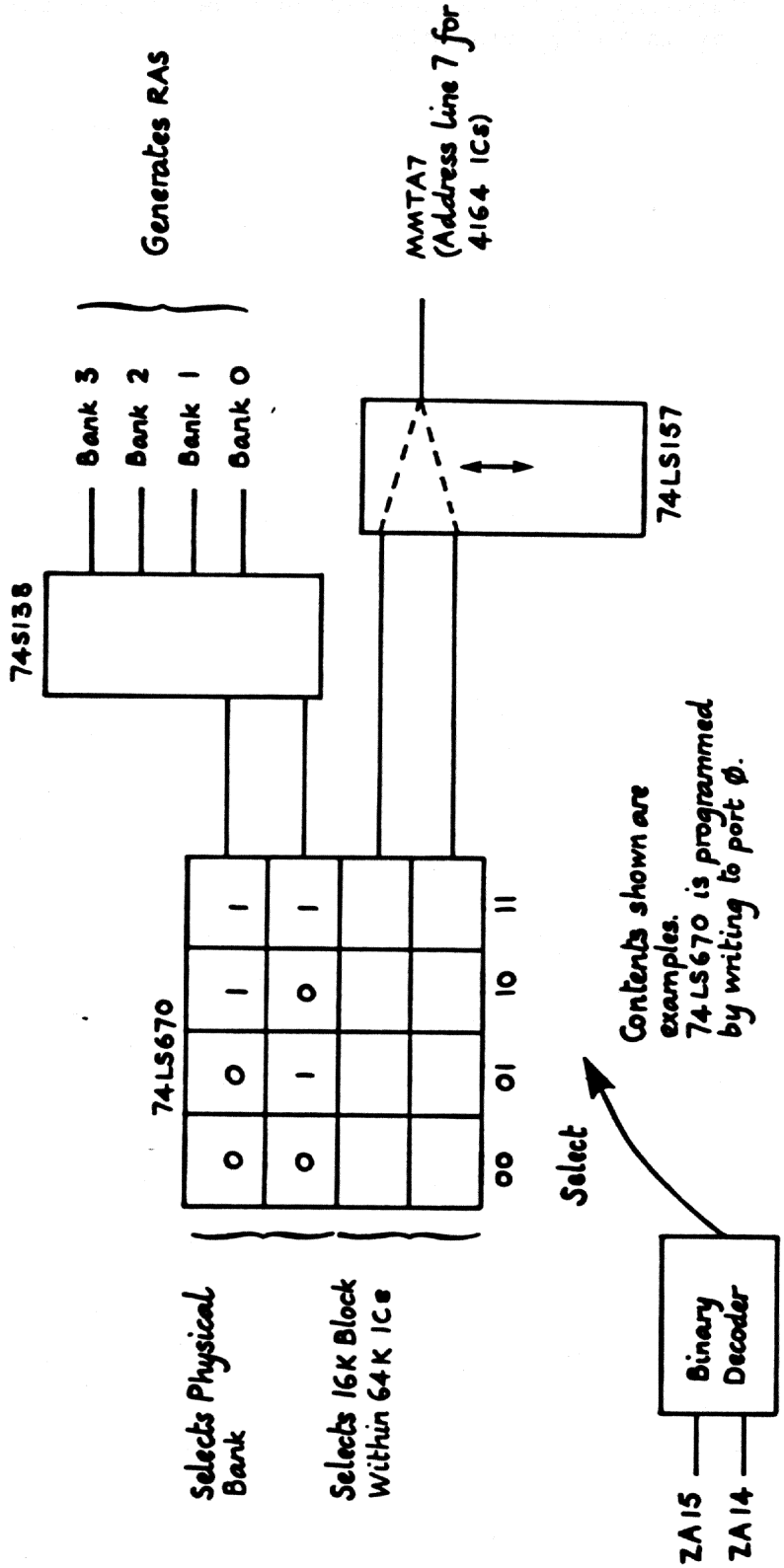

Figure 2.3 RAM Mapping

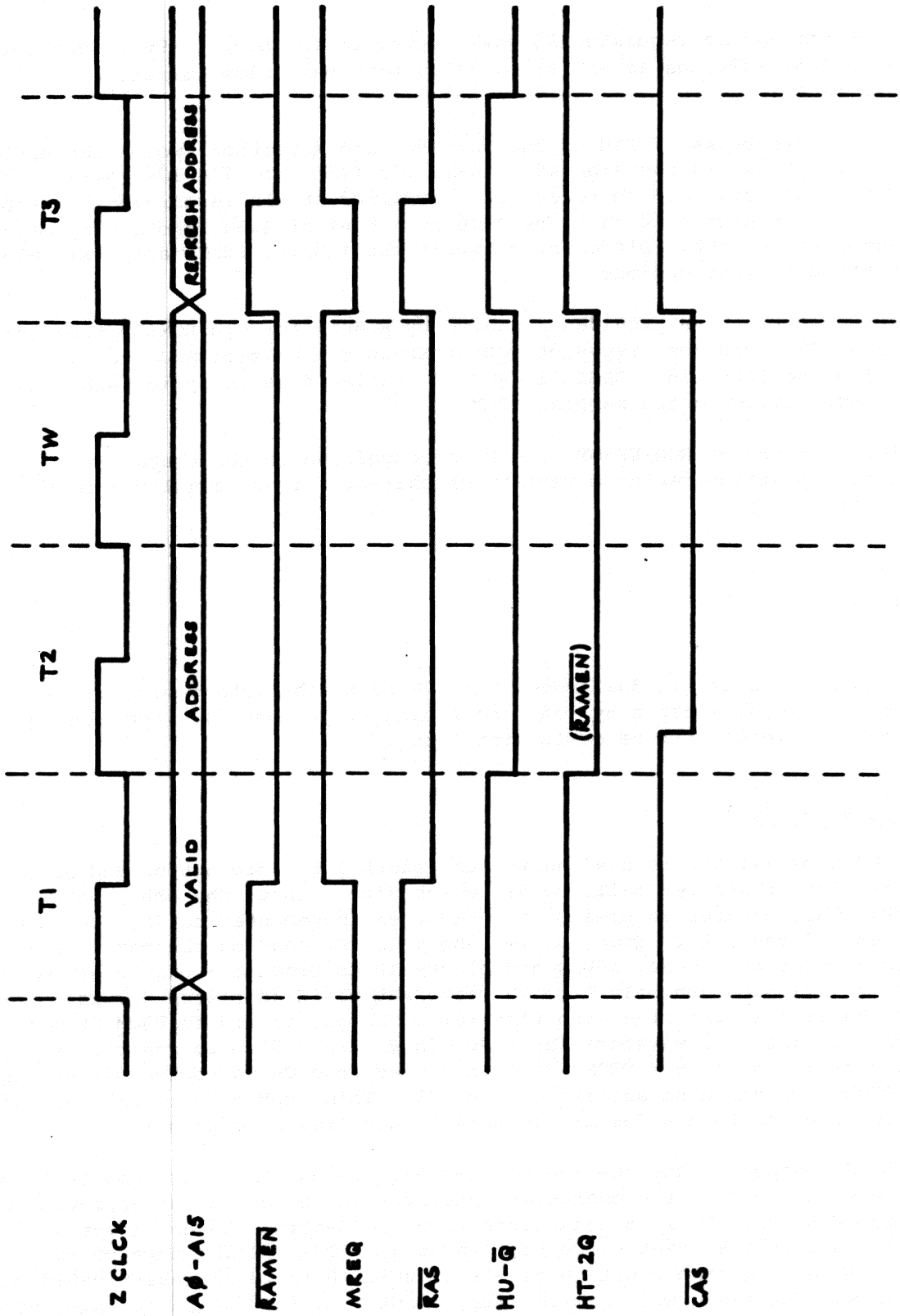

Figure 2.4 RAM Access Cycle

SHEET 3

This describes the regulated DC power entry to the board: +9V is developed onboard from +12V, as is -5V from -12V, both being low current requirements.

There are two banks of RAM on the main PCB and a further two on the option PCB. Each bank can contain either 4116 ICs (16K) or 4164 ICs (64K), and link pads are provided to cater for the different pin requirements. A 64K system may consist of 4 banks of 4116 or 1 bank of 4164, and memory may be expanded up to 256K. Different firmware and mapping PROMs are available to suit the different options.

Four ROM sockets are provided, enabled by ROM0EN through ROM3EN from the mapping PROM, and most types of ROM or EPROM can be accommodated by altering the link pad. BASIC in ROM is available as an option with its associated firmware and mapping PROM.

A similar range of ROM/EPROMs can be accommodated in the character generator position making a variety of character fonts available to the video circuitry.

SHEET 4

The video circuitry is dual mode, i.e. 40 or 80 characters wide by 24 lines. It is selectable by software (using write port 2). For clarity, 80-character mode will be dealt with first.

80-Character Mode

The 16MHz oscillator is used as the dot clock for video output and is divided into character cells by JP, which also outputs the 4MHz system clock. This counter is preset to 8 and then incremented to 15, whereupon EOC (end of character) goes active, and 8 is reloaded on the next clock pulse. EOC occurs every 500ns and clocks IP to produce a character count of 0 to 127, although only 0 to 79 represent valid addresses. This count takes 64ns, i.e. one line scan time for a VDU and is fed to PROM GR which 'maps out' the line waveform (as shown in Figure 2.5). To restrict the number of lines of this PROM, C0 is not used, and C6 is routed via HP i.e. the PROM receives even addresses 0 to 126. This PROM outputs LBLNK to give a blank area on both sides of the screen, and line sync pulses.

The LCLK1 output clocks the row counter HR, giving line slice counts 0 to 9. These are fed to the character generator IC to select the appropriate character slice. R3 is a convenient waveform (active 128 us, inactive 512 us) for use in the reset circuitry (sheet 1). The falling edge of R3 clocks IQ giving line counts 0 to 31, of which 0 to 23 represent valid data addesses. The field waveform is 'mapped out ' by PROM HQ in the same way as the line waveform. Output FBLNK1 blanks scan lines between text lines by

inhibiting $\overline{\text{LOAD}}$ to the shift register, and FSYNC1 is the separate field sync output. FS is fed back to GR which, in combination with LSYNC1, generates mixed sync (MSYNC) and is used to produce the composite video output. Field RESET (FR) is used to 'trim' the field time to the required 20ms (50Hz) by resetting and row counters during line count 31. If these were not reset, the field time would be:

32 (max line count) x 10 (max row count) x 64us (line time) = 20.48ms

which might cause instability.

During normal screen refreshing, the 7 character-count bits (C0-C6) and 5 line-count bits (L0 - L4) define the character position in RAM with some redundant addresses. The 2K RAM used, although being of adequate capacity for the display, only uses 11 address lines (with no redundancy) and is not compatible with the 80 x 24 screen format - in other words the RAM is 'too square' - and so some juggling of address space is needed. In 40-character mode no problem arises, but in 80-character mode addresses greater than 63 are mapped down to the redundant lines (24 to 31) in three groups because CC6E is active (column count C6 via GP and HP) and switches the multiplexer, MP. This is illustrated in figure 2.6.

Access to the video RAM is divided into two equal time slots by the 2 MHz signal VDUACC/$\overline{\text{CPUACC}}$ so that the CPU can write to the screen without any timing restrictions and without disrupting screen refresh. During screen refresh (VDUACC high) the character and line counts are selected by the multiplexers KP, GQ, and GP, and are latched into LP, MP, and KP on the falling edge of 4 MHz (i.e. half-way through VDUACC). When EOC is active, the data addressed is latched into MQ on the rising edge of 16 MHz (i.e. half-way through $\overline{\text{EOC}}$) and is presented to the character generator. At the same time, the outputs SR0 to SR7 from the previous character are loaded into the shift register JQ, provided that valid data exists (i.e. LBLNK and FBLNK are inactive). This data represents the dot format of the selected character slice, and is shifted out at 16MHz as VIDEO. Figure 2.7 shows the timing.

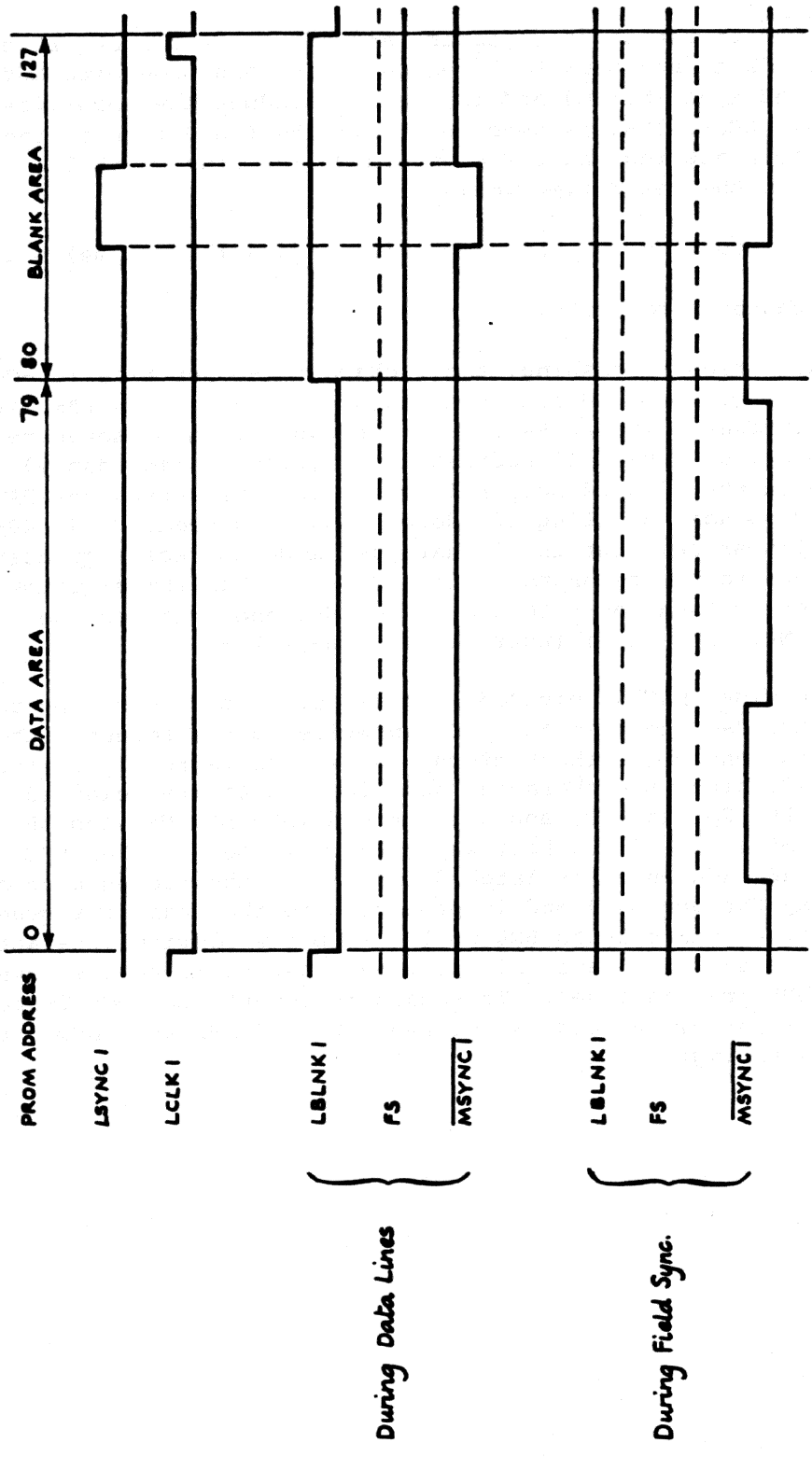

Figure 2.5 Line Waveform

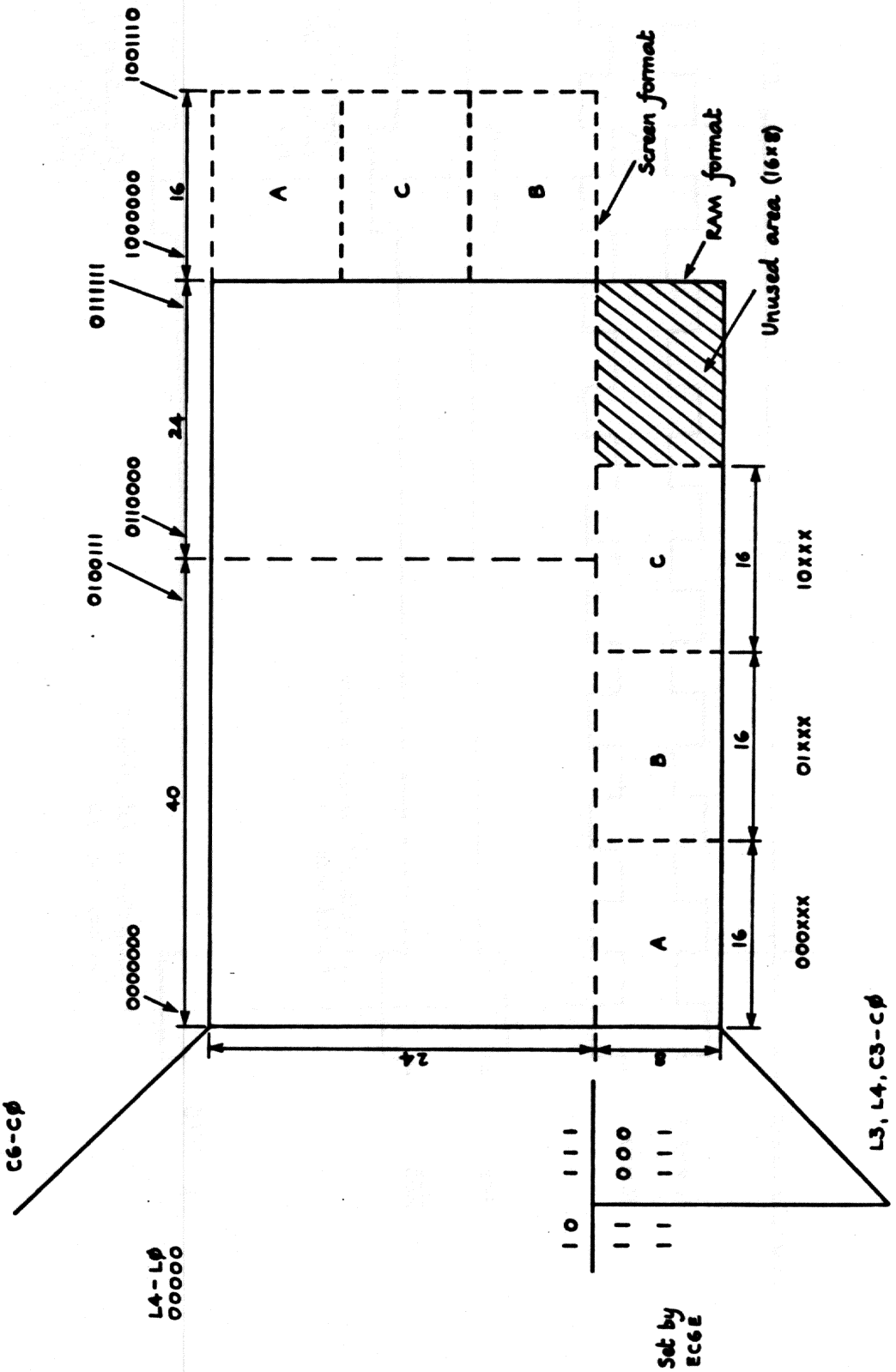

Figure 2.6 Video RAM

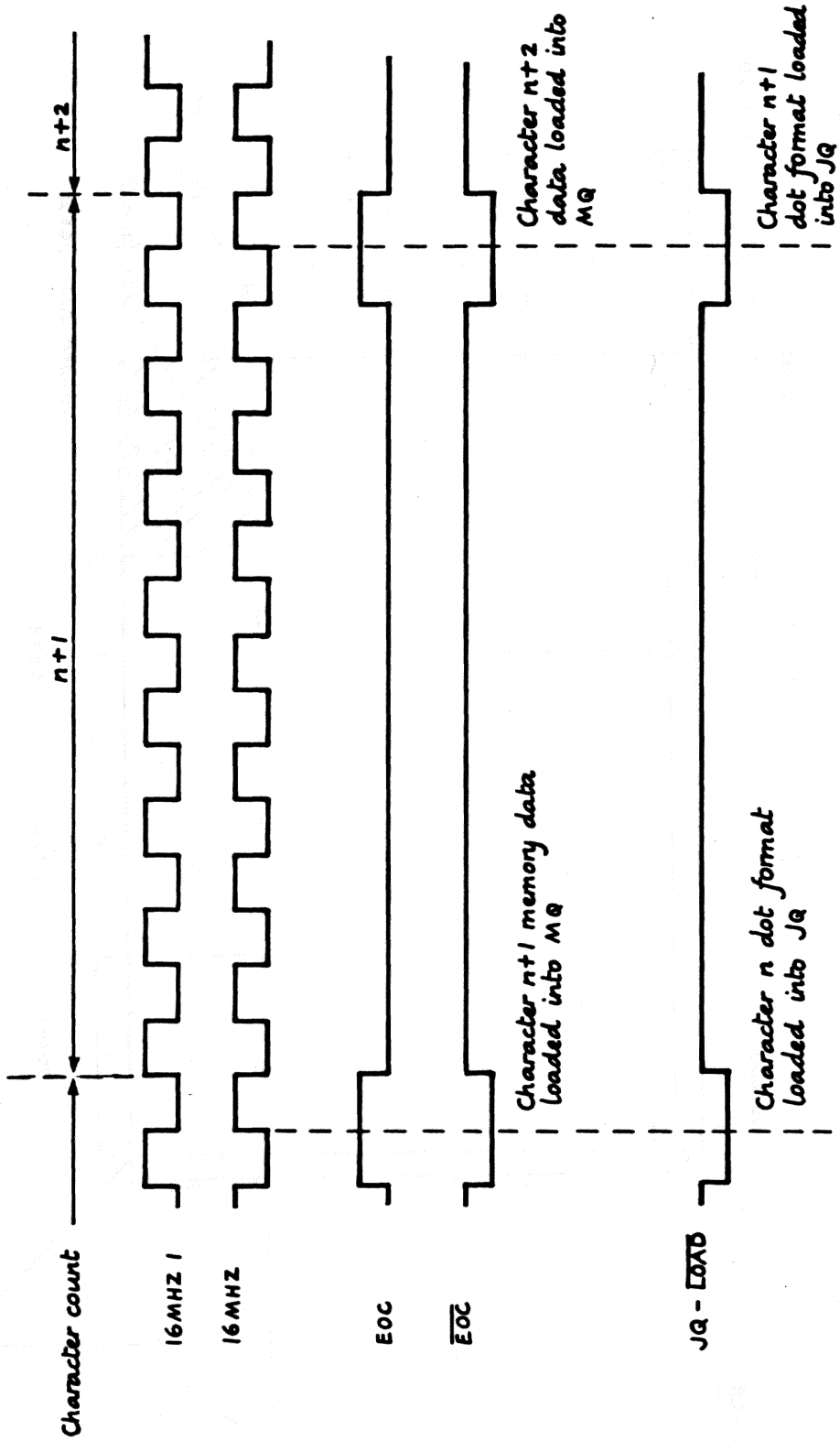

Figure 2.7 Video Timing

The CPU writes to video RAM by means of an OUT (C) instruction using ports 0 to 17H, i.e. one port for each of the 24 display lines. An output instruction has one wait state inserted by the Z80, and one additional wait state is inserted by VDUEN (sheet 1). This ensures that a valid address on the bus during the instruction is coincident with the falling edge of 4MHz during CPUACC, and is latched into KP, LP and MP. LP also latches the VDUWR signal to allow data on the M bus (latched during CPUACC - sheet 1) into the RAM. During the instruction, A0 to A6 contain the port number (i.e. line number) from register C; A7 to A15 contain the character number (from register B) and the data bus contains the character (from register A).

The CPU can read the contents of video RAM in a similar way using IN (C) instructions.

40-Character Mode

In 40-character mode, the counter JP is preset to 0 and so EOC now occurs every 1us, giving twice the character width of 80 mode. C6 is not used, and so IP outputs counts 0 to 63 in the 64us line time. C0 is gated to the line PROM GR (via HP) and a different map is used (80/40 high) to allow for the different inputs. The frequency of the least significant bit of the count on GR (C0 or C1 depending upon screen width) remains the same at 1 MHz. The remainder of the counting circuitry works the same as in 80 mode, and, as no juggling of RAM space is now necessary, CC6E is disabled by HP. In this mode the shift register JQ is inhibited on each alternate clock to give a half-speed dot rate.

The various video signals generated on this sheet are mixed at the base of TR1 to produce a composite video signal. Separate sync signals are made available. VIDMIX2 comes from the high resolution graphics circuitry on the option PCB and allows mixing of text and graphics on one monitor - this can be disabled by software. DIM1 indicates that the character displayed is one of the grey graphics symbols (70 - BF H) and reduces the amplitude of the video signal. A modulator is also included to produce a UHF output.

SHEET 5

This sheet shows all of the system ports except write port 0 (the mapping register - sheet 2). The group is selected when PORTEN is active and the separate ports are decoded - sheet 1. Data transfer is via the 'T' bus which is enabled by TDBUSEN at the same time as PORTEN is active.

Read Ports

Read ports 0, 1, and 2 are 74LS244 buffers enabled directly onto the bus and are thus time dependent.

- Read port 3 is a latched port used for keyboard data. KBDSTB clocks data into the latch and generates KBDREADY which inhibits further data strobes from the keyboard. KBDREADY is available as a status bit in read port 1. KBDSTB1 goes to the CTC (sheet 6) to generate a program interrupt. The monitor program reads the data during the interrupt service routine and stores it in a buffer area of main memory for later use by the user program. Reading port 3 clears KBDREADY and allows the keyboard to send further data.

- Read port 5 is also a latch and is used as the parallel input. USTBIN clocks data in, generating UINRDY which is available as a status bit in read port 1 along with its associated handshake UHIN1. INRDY is a status signal, going back to the inputting device, which goes 'low' while data remains in the latch and is reset to a 'high' when the port is read.

Write ports

Write ports 1, 2, and 5 have latched outputs.

- Port 5 is used as parallel output with its associated handshaking signals UHOUT1 - 3 from write port 1. Write ports 1 and 2 contain various control signals, all of which are cleared during reset. This is important as the keyboard must not be allowed to generate an interrupt until the CTC has been set up, and so KRESET remains 'low' until changed by the initialization firmware. Another important part of the power-up procedure is that PAGE 0 and PAGE 1 are 'low' to enable the Z80 to fetch its first instruction from ROM0 at address 0000 (memory mapping - sheet 1). During initialization this is changed so that RAM is addressed at the bottom of memory. NMIEN is used by the monitor for single stepping through programs and enables an NMI to be generated (sheet 1). 80/40 selects the screen format and ALTCHR goes to the character generator (sheet 4) to select one of two fonts. Write port 5 is a DAC, the output of which can be connected to the loudspeaker (sheet 6) and is available as ANALOGOUT. The SIO2 interface is software controlled using port 2 (read and write).

CR provides an interface for joystick potentiometers (for games etc.). The monostables are triggered by the program via HTRIG (write port 2) and

generate pulses JT1 and JT2 which are proportional in width to the position of the joystick (i.e. value of resistance). Both outputs can be monitored by the program using read port 2.

SHEET 6

The SIO is set up during initialization so that channel A is used for the network interface (this requires a network transceiver board to interface to the coax). Channel B is set up by the monitor program as the SIO4 interface and it has several baud rate options.

The CTC ports are set for the following use:

Ch0: This is clocked at 2MHz, and is used either as the SIO4 TX/RX clock, or as a timer for detecting the frequency of cassette input.

Ch1: Has three uses: to detect edges on cassette input (the time between edges then being measured by Ch0); to generate cassette output frequency; and to time output for the SIO2 interface. These three functions are mutually exclusive.

Ch2: Is used purely to generate interrupts from KBDSTB1.

Ch3: Clocked at 50Hz (field blanking signal - sheet 4); this channel is enabled when the repeat key is pressed to generate interrupts at the repeat frequency.

Interrupt daisy chain is such that the SIO has top priority (for network use) with the CTC second. The option PCB has lower priorities.

When writing to cassette, the output of CTC Ch1 is divided by two and fed through an op-amp filter circuit to produce an approximate sine-wave suitable for cassette recorder input. Signals from the recorder are fed to two op-amps: the first checks the amplitude against a reference and outputs signal CASVOL to read port 2 if the volume is insufficient for reliable reading; the second one squares the sine-wave input to give a TTL signal CASIN on read port 2.

Another amplifier circuit is included to drive the internal loudspeaker. This is fed by LSPEAK (write port 2) enabling the program to generate a tone in the speaker. The amplifier can also be fed from the DAC (sheet 5) to produce sounds at various intensities.

SECTION 3

OPTION PCB

(Circuit ref. : D10830, Sheets 1 to 5)

SHEET 1

The two extra banks of RAM sockets are shown which, as with the main board, can be linked to accept either 4116 or 4164 ICs. This allows memory to be expanded to 256K.

High Resolution Graphics

An extra 16K block of memory is included on the option PCB which is dedicated to graphics. This is configured as 192 rows, each with 80 bytes, and allows pixels to be plotted on the screen using X and Y coordinates. The HRG memory is separate from main memory and is accessed via the HRG ports (4 read and 4 write). There are three levels of resolution, selectable by software:

1. Extra High Resolution

   In this mode each of the 80 bytes per row represents 8 pixels, giving 640 (horizontal) x 192 (vertical) pixels on the screen. Each pixel can have only two possible values: 1 (white) or 0 (black).

2. High Resolution

   In this mode each byte represents 4 pixels (2 bits each); this gives only 320 (horizontal) x 192 (vertical) pixels on the screen. However, each one now has four possible values.

3. Medium Resolution

   This mode uses 4 bits per pixel, each having 16 possible values. Vertical resolution is also halved, giving 160 (horizontal) x 96 (vertical) pixels on the screen. This only uses half of the 16K memory and so two 'pages' are available, allowing the CPU to modify one page while the other is being displayed.

In modes 2 and 3 the pixel 'value' goes to a lookup table which is programmed by software. This is a 16 x 8 register and allows each pixel value to be converted to any 8-bit value from 0 to 255. The output is passed to a DAC to give the desired pixel intensity which can then be mixed with text on the normal black and white monitor output. Three bits of the lookup table output are also passed to the RGB output driver, allowing the use of a colour monitor. As with the black and white output, text can be mixed with graphics under software control. The three 'colour bits' chosen from the eight bits are those which will give a sensible relationship between colour and intensity. Although sixteen intensities are possible in

medium resolution, only eight colours can be displayed on the RGB output (TTL levels).

SHEET 2

HY buffers the 'Z' data bus to the 'I' data bus when accessing the HRG ports (HRGEN active). The direction of data is controlled by RD. CT is also enabled at this time and decodes the lower two address lines to strobe the appropriate HRG port (RD0 - RD3, WR0 - WR3). CP keeps data stable in HY until the next rising edge of 4MHZ, after HRGEN and WR go 'high', allowing the rising edges of WR0 - WR3 to be used as strobes.

When writing to HRG memory, the CPU puts the Y address out via WR0 and the X address out via WR1. These are latched into FW and GR respectively. During line blanking, VMEME is low putting the latched X and Y addresses through to the memory, at which time the CPU can put pixel data out through WR3. Whenever HRG port 3 is accessed CRAS goes active (giving MRAS via EQ); the next rising edge of 4MHZ puts CAM and MAM 'low' to switch the address line multiplexers GQ and FT. After a short settling period governed by R11/C1, MCAS goes active to enable the RAM data lines. (Timing is shown in figure 3.1.) During memory writes, WR3 is active putting VMR/W (memory read/write line) 'low' via EQ. During memory reads, DW is enabled by RD3 putting memory data onto the 'I' bus.

The 16K RAM is not directly compatible with the 80 x 192 format used in this circuit, and has to be configured in a similar way to the video RAM on the main PCB. This function is performed by ET which re-positions columns 64 to 79 (i.e. C6 is active). Figure 3.2 shows this action.

During normal screen refresh counter EU is clocked by 2MHZ to give the column, and is reset by VMEME at the end of each line. FR is clocked by LCLCK and reset by FRESET (both from the main PCB) to give a line count which is synchronized with the normal text output. The column count goes to the memory via FU and the line count goes via FS; both are enabled by VMEME. In medium resolution all even lines are page 0, and all odd lines are page 1. In this mode LC01 is set by the state of FORCE (i.e. page select) via EP, thus reading alternate lines of memory on two consecutive scan lines. VMR/W is set high by EQ (VMEME high) to disable writing, and VRAS is developed by the HRG timing chain (sheet 3). The address line multiplexers (and subsequently MCAS) are switched by 2MHZ from the timing chain.

HRG port 2 is used for control and status:

OPEN	stops screen refreshing and allows the CPU unlimited access to memory (dynamic RAM refreshing is the responsibility of the CPU during this time).

VSCALE and $\overline{\text{HIRES}}$ set the mode of operation:

	VSCALE	$\overline{\text{HIRES}}$
Extra high resolution	0	0
High resolution	0	1
Medium resolution	1	1
Not valid	1	0

$\overline{\text{FORCE}}$ sets the page to be displayed in medium resolution.

$\overline{\text{VIDINH}}$ inhibits text on the RGB output.

$\overline{\text{HRGINH}}$ inhibits graphics on the black and white output.

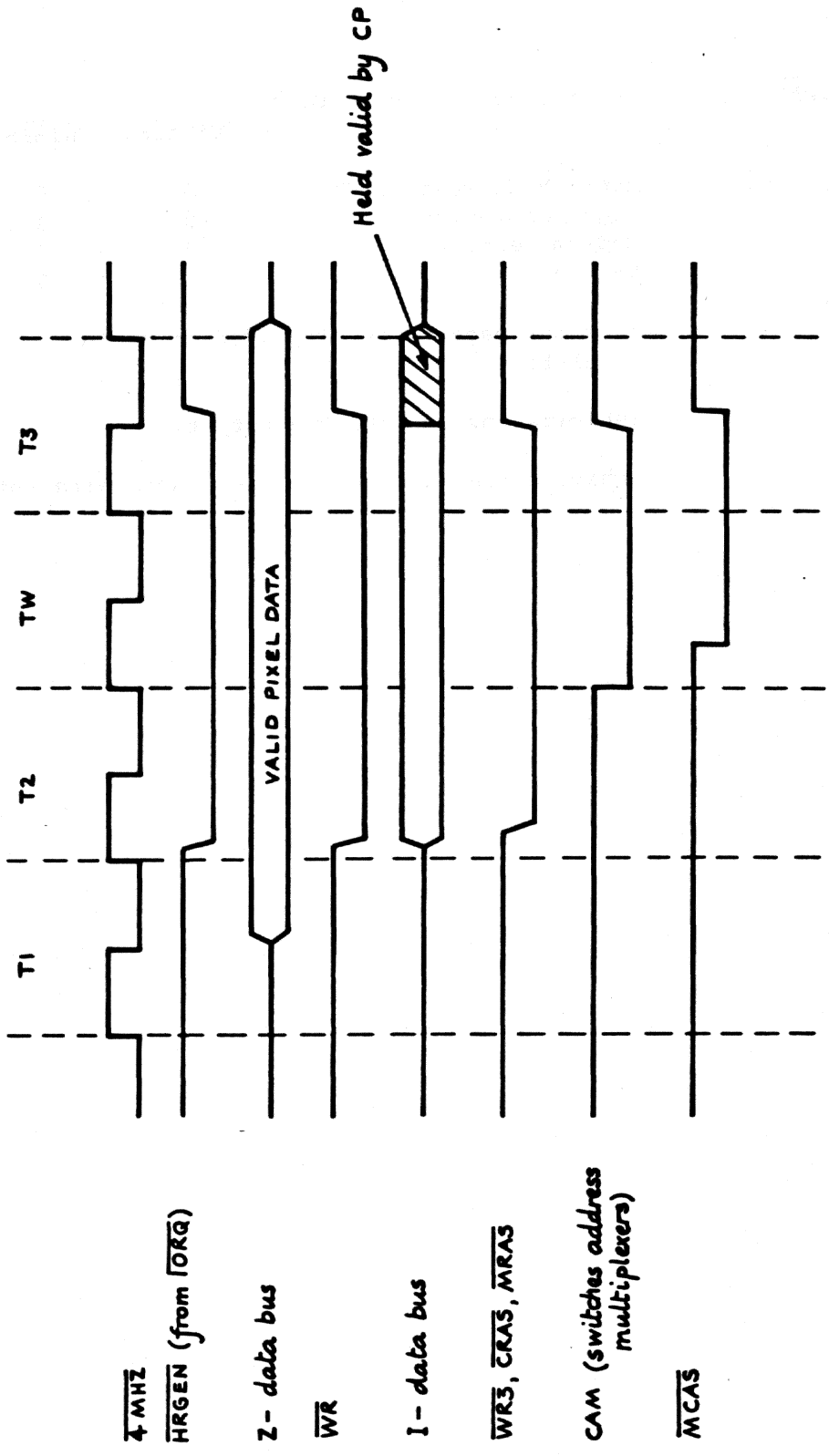

Figure 3.1 Writing to HRG Memory

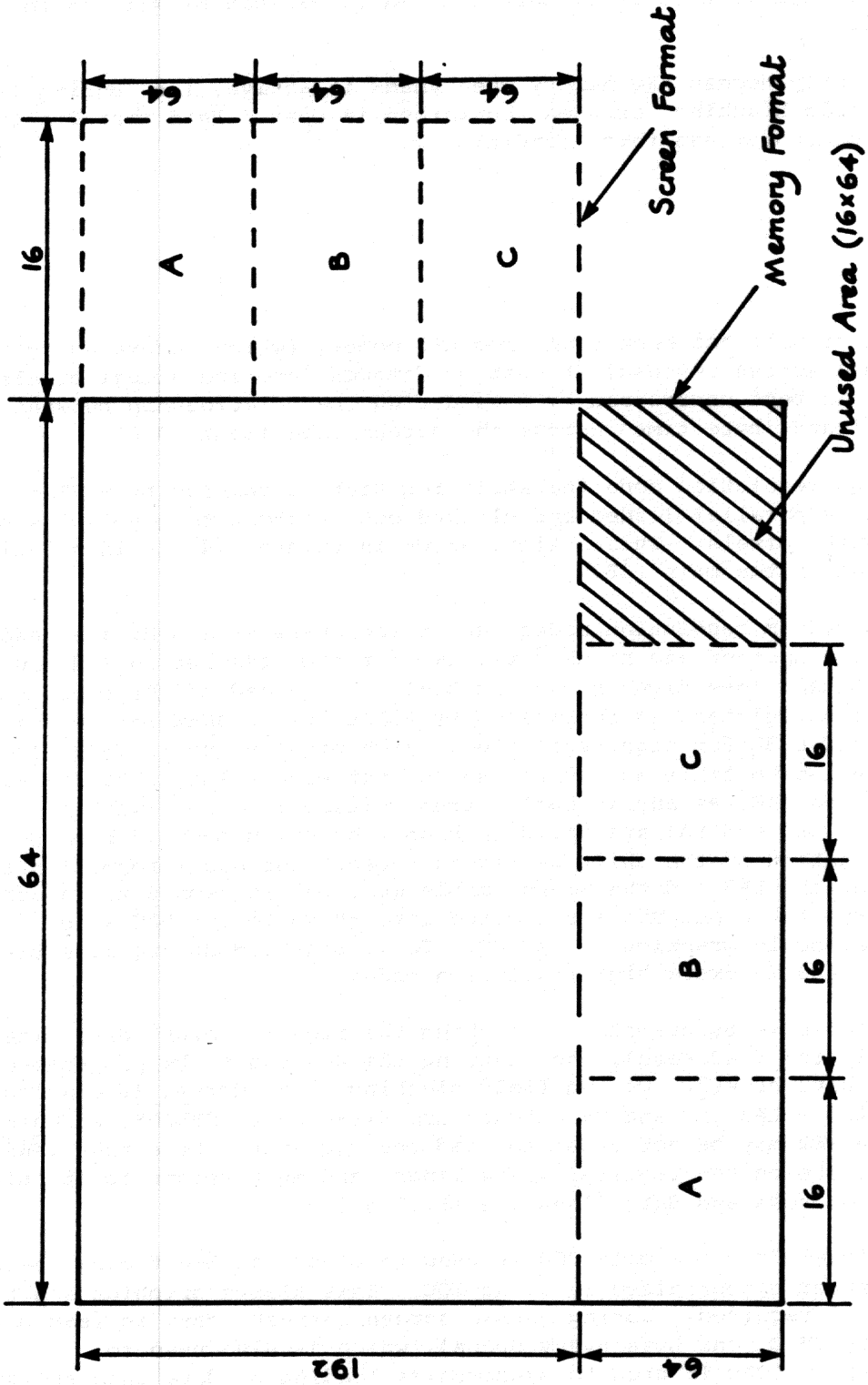

Figure 3.2 Memory Re-mapping (HRG)

During field blanking, ID0 to ID3 are enabled through to LA0 to LA3. If LKWR is activated at this time, data latched in WR0 can be written to the lookup table.

The CPU can only access HRG memory when VMEME is active, i.e. during line blanking, field blanking, or when the screen is open. Read port 2 allows the CPU to monitor these three conditions.

SHEET 3

Once a byte of data has been read from HRG memory (which occurs every 500ns during normal screen refresh) it must be divided into individual pixels. This action is best understood by considering the relationship between 'pixel time' and 'byte time' across the screen (see figure 3.3).

In extra high resolution mode the shift register is enabled by HIRES; memory data is parallel loaded and clocked out at 16MHz to give a row of black and white pixels. This action, shown in figure 3.4, is identical to 'text' output on the main PCB.

In high and medium resolution modes, shift registers EV and DV are used to 'pick out' the appropriate pixel bits: two for high resolution and four for medium resolution (see figures 3.5 and 3.6). The speed of the clock going to these shift registers is controlled by VSCALE using 4MHZ for medium resolution and 8MHZ for high resolution. Each pixel value is input to the programmable lookup table as LA0 to LA3 so that each value (0 to 15) may appear, via the DAC, as any intensity from 0 (black) to 255 (white). Although only LA0 and LA1 are valid in high resolution mode (2 bits per pixel), the action of the shift registers causes spurious information to appear at LA2 and LA3 and the lookup table must be programmed to ignore these. Lookup table outputs are clocked through ES to the DAC which produces grey-scale graphics at DACOUT. ES is disabled during line blank, field blank, and in extra high resolution mode.

The lookup table is programmed by latching the required eight data bits in WR0 (normally the Y address), then setting the address to be programmed in the lower 4 bits of WR2. During field blanking this address is enabled through to LA0 - LA3 (EV and DV outputs are disabled by FBLANK) at which time LKWR in WR2 may be activated to load the register. Note that LKWR is used as a strobe on the register write lines, and must return to its high state while address and data lines are still valid.

The 16MHz signal from the main PCB is used to clock the HRG timing chain, which is further synchronized by using EOC. This allows graphics and text to be mixed if required. During normal screen refresh, data is read out of HRG memory by 2MHZ (one byte every 500ns), which is also used to generate VRAS. HLOAD is used to synchronize loading of data into the shift registers. The line-blanking signal (LBLNK) is taken from the main PCB and used to generate VMEME, the signal which enables the CPU to access HRG memory. In 80-character mode, VMEME is delayed by two extra clock pulses, again to provide text/graphics synchronization. FBLNK from the main PCB is

gated with LC6 and LC7 to give $\overline{\text{FBLNK}}$ and is used to reserve the bottom area of the screen (scan lines 192 - 239) for text only. $\overline{\text{BLANK}}$ is a derivation of $\overline{\text{FBLNK}}$ and is used to disable the lookup table outputs (high and medium resolutions) during line and field blanking; this signal is always in extra high resolution mode.

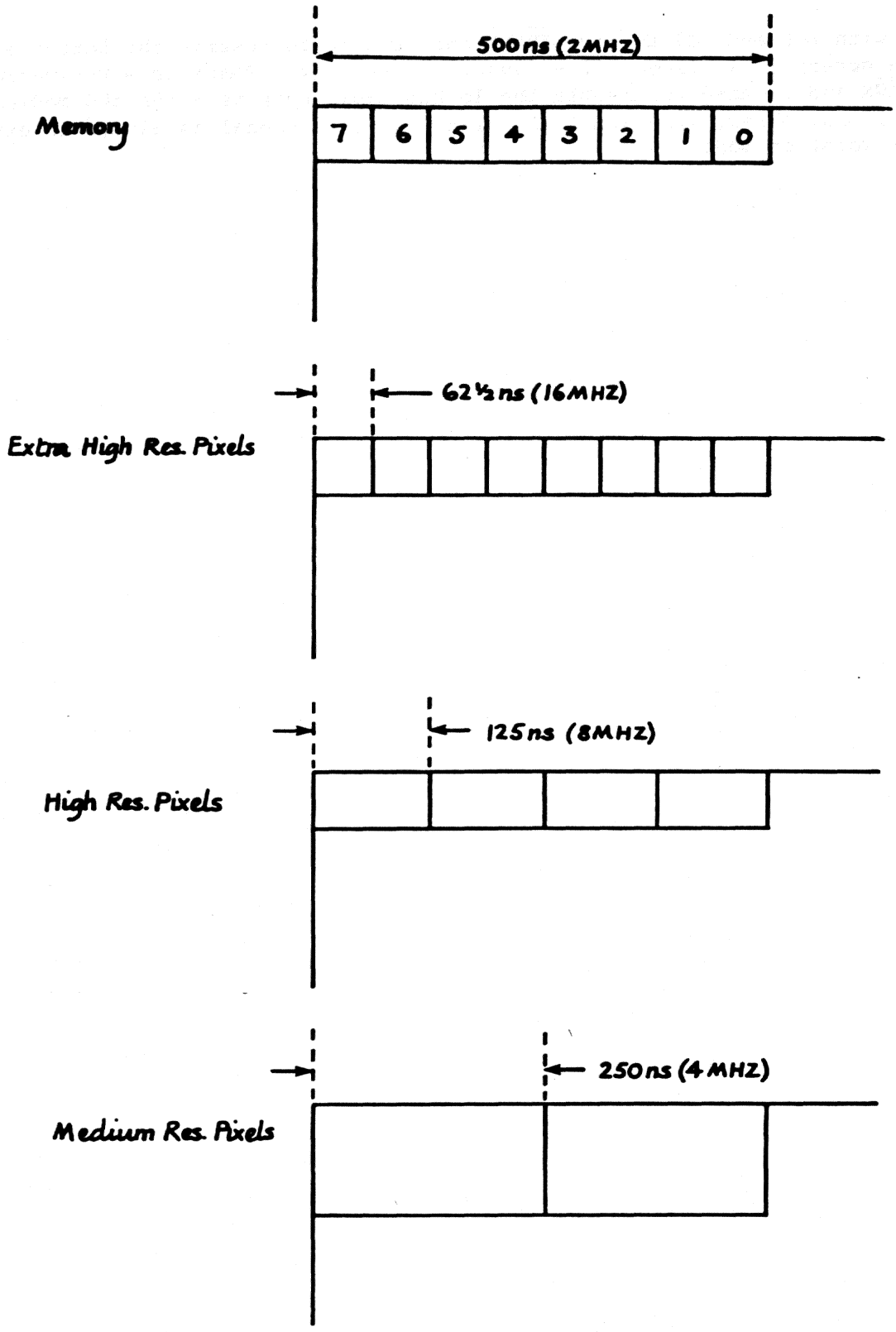

Figure 3.3 HRG Modes

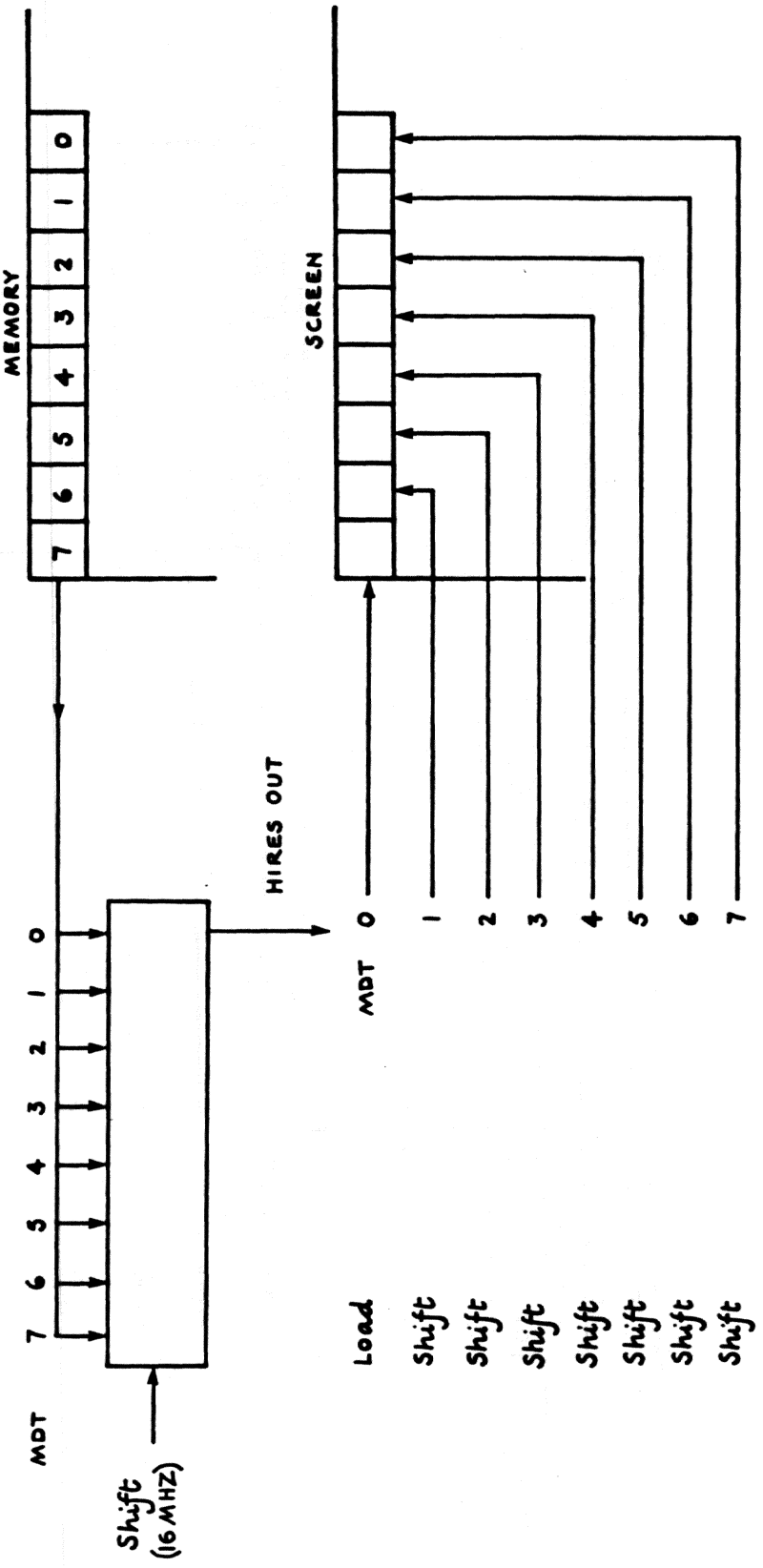

Figure 3.4 Extra High Resolution

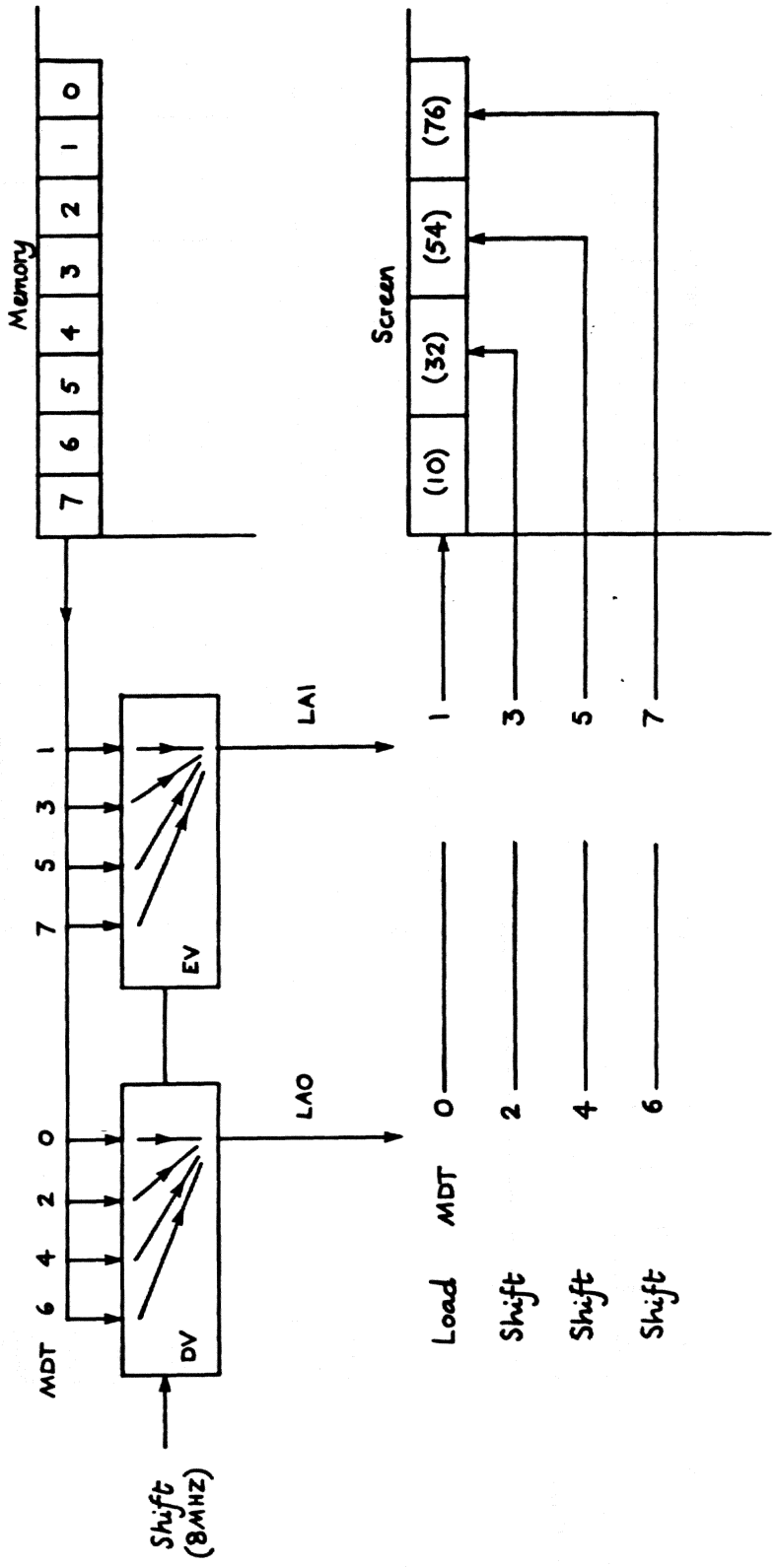

Figure 3.5 High Resolution

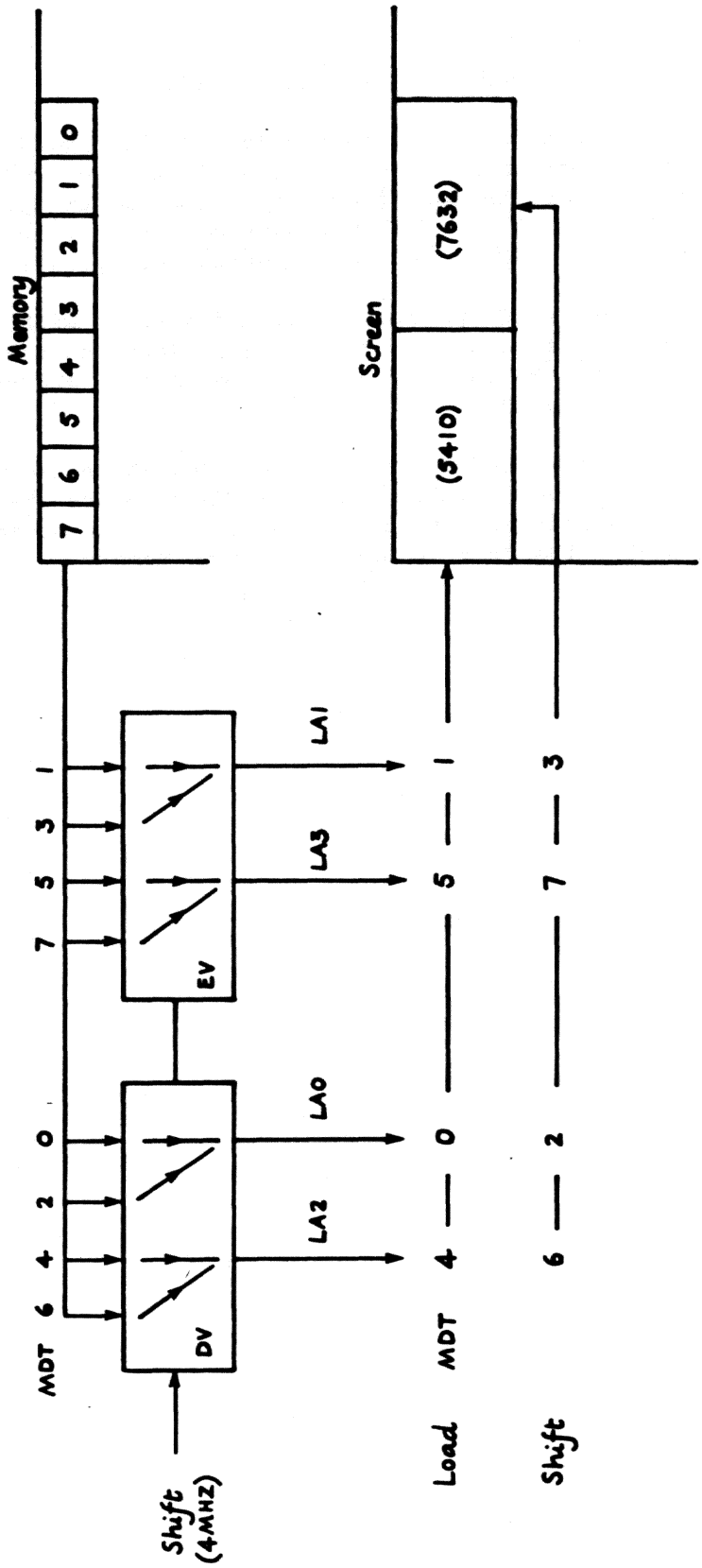

Figure 3.6 Medium Resolution

SHEET 5

This sheet shows two dedicated ICs and a CTC:

- BS is an IEEE interface controller, enabled by $\overline{\text{IEEEEN}}$ from the main PCB for programming, and provides all the control functions necessary for the interface. Processor interrupts are generated via the CTC channel 0. The IEEE address can be read as a status in HRG port 0 (RD0). AQ and BT are interface buffers.

- BU is a maths IC, providing maths functions with a minimum of software. Processor interrupts are generated via CTC channel 1. The $\overline{\text{CTC/9511 EN}}$ is a shared group of ports, and chip select is controlled by A2.

- CTC channels 2 and 3 are used as a real-time clock: Ch.2 provides interrupts every 8ms if required; Ch.3 counts the outputs of Ch.2 to generate interrupts at 1 second intervals so that the processor can update the 'time counter' in main memory.

SECTION 4

POWER SUPPLY

GRESHAM LION TYPE 32047

(This is a copy of the technical description supplied by Gresham.
Circuit ref. : Gresham Lion Drawing No. 320470/1/030)

GENERAL

The mains input is rectified and smoothed to give a nominal 320V d.c. supply. This powers a single transistor flyback converter operating at between 30 kHz and 100 kHz depending on output loading. Regulation of the main 5V rail is achieved by opto-coupler feedback controlling the 'on' time of the converter, while the +12V and -12V rails are controlled by 'low-drop' series regulators.

MAINS FILTER AND RECTIFIER

RFI generated by the power converter is suppressed by the mains filter (C12, T1, C1, C2, and C3) which reduces the RFI to below that required by BS800. R1 is included as a discharge path for C12 and C2. The mains input, which is isolated by SW1 and protected by FS1, passes through THT1 (a 70°C thermal output); it is then rectified by D1 - D4 to give 320V d.c. (nominal) on C4 and C5. Resistor R13 limits the switch-on surge as C4 and C5 are charged initially. The series choke, L2 and C5, filters the switching frequency current and reduces the high-frequency noise reflected into the mains supply.

FLYBACK CONVERTER

At switch on, R7 provides bias to TR3 which starts to turn on. Positive feedback via T2 (pins 11, 12), R11, R2, D7, and D8 turns TR3 on fully and the current through TR3 rises linearly from zero as energy is stored in the core of T2. To prevent TR3 from saturating, D11 conducts when the collector voltage of TR3 approaches 1.5 volts and diverts current from the base of TR3 so that the collector voltage remains at 1.5 volts during the 'on' period. TR3 collector current flows through R9 and causes a voltage ramp to appear at the emitter of TR2. The voltage level at TR2 base is set by R8 and by the current flowing through the transistor of OC1; when the voltage at TR2 emitter exceeds this level by more than 0.6V (approx). TR2 is turned on causing TR1 to turn on. Base current is drawn from TR3 via D6, causing TR3 to turn off. As TR3 turns off, positive feedback via T2, R11, R2, D9 and D10 keeps TR3 off. The negative voltage

applied to D5 cathode charges C65 to provide a negative auxiliary supply which is used to turn off TR3 and bias TR2 base.

As TR3 turns off, its collector voltage rises until it is clamped by the secondary windings of T2. Shortly after TR3 turns off, TR2 turns off due to lack of signal input and the charging of C9. TR1 then turns off as well and C9 resets to its normal level ready for the next turn-off sequence. The collector of TR3 remains 'high' until all the energy stored in the core of T2 has been discharged into the secondary circuits. When this is complete, the collector voltage of TR2 starts to fall at a rate determined by the snubber components and the primary inductance; when this voltage is equal to the supply voltage, a new cycle is initiated via R7 (as before).

If there is no feedback signal via OC1, the peak current at which turn off occurs is determined by the voltage on the negative auxiliary rail, which (in normal operation) is approximately equal to the breakdown voltage of Zener diode D12. When turned on or off, and under secondary short circuit conditions, the voltage on C6 is reduced due to decreased drive from T2. The peak collector current is therefore reduced to ensure reliable operation under all conditions.

SNUBBERS

When a high voltage power transistor is turned off it is necessary to ensure that the collector current falls to zero before the collector voltage has reached a critical value (approximately 400 volts). This is accomplished by diverting the current which is flowing in the primary inductance of T2 into C10 via diode D13; R10 allows C10 to be discharged without subjecting TR2 to a high pulse loading. At turn off, the collector voltage of TR3 could rise to a high value due to the leakage inductance between the primaries and secondaries of T2 but this is prevented by a clipping circuit D22, R12 and C11. The voltage on C11 is approximately constant during each cycle at the required maximum TR3 collector voltage. If the voltage exceeds this value, D22 conducts and the resultant energy stored in C11 is partly fed back to the supply and partly dissipated in R12.

SECONDARY OPERATION

When TR3 turns off, all the secondary diodes conduct and pass the energy stored in T2 to their respective capacitors, C104 etc. Because these windings are closely coupled, the voltages on the capacitors are proportional to the turns ratio of the secondary transformer windings. The 5-volt rail voltage is monitored by IC1 via R104. IC1 contains a reference of 7.1 volts (nominal) on Pin 6 and this reference is divided by RV101 and R105 to give 5 volts at Pin 4, the inverting input of an amplifier. Pin 5 is the non-inverting input and Pin 9 is the output of

this amplifier. If the output voltage is low the output of IC1 will be low and the current in OC1 will be low. This gives rise to an increase in output power which tends to correct the initial error condition. R102 and C101 are compensating components which stabilise the loop.

Inductors L101 and L102 are part of P1-type output filters which reduce the high frequency ripple at the output terminals. TR101 and TR102 are the series-pass transistors for the regulators on the +12 and -12 rails respectively. These are driven by their associated op-amp which compares the rail output voltage with the 5-volt output and adjusts the drive to the series transistor to maintain the required output voltage.

In the event of the voltage on the 5-volt rail exceeding 6 volts (approximately), Zener diode D108 conducts and provides gate drive for SCR101; SCR101 turns on and 'crowbars' the 5-volt output, blowing fuse FS102 and removing the 5-volt (and +/-12V) output.

SWITCHING PSU LOAD BOX

Function To provide an effective load on the PSU for testing and repair without the risk of having the main circuitry connected.

Loads on each rail are switchable between typical and maximum loads.

Test points are provided to quickly check the voltage of each rail, and current drawn.

PSU Spec.

RAIL	TYPICAL LOAD	MAX. LOAD
+5V	2.5A	3.5A
+12V	0.25A	0.82A
-12V	0.05A	0.1A

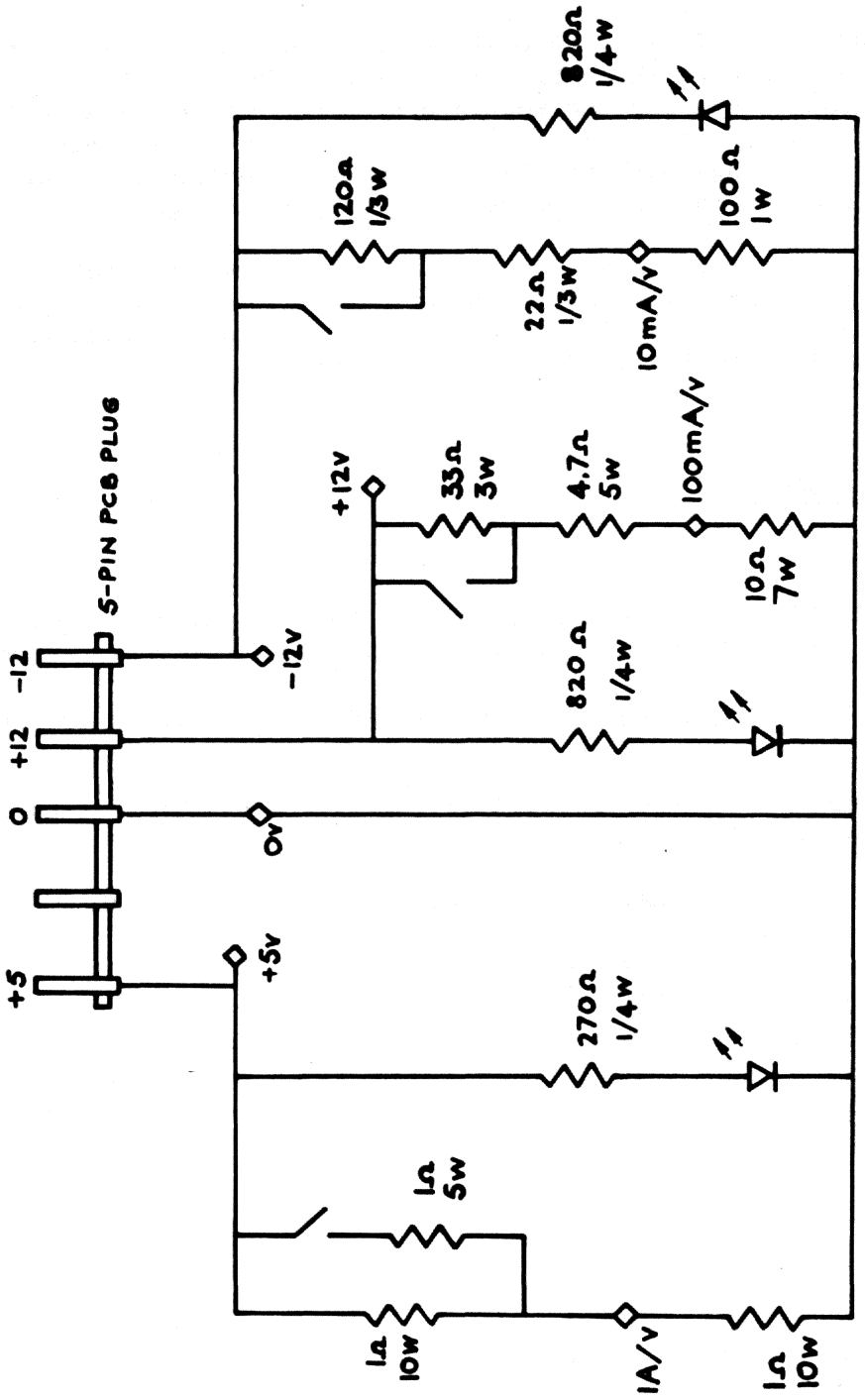

Figure 4.1 Power Supply

480Z FAULT DIAGNOSIS GUIDE

CONTENTS

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SECTION 2	BRIEF CIRCUIT DESCRIPTION	2.1
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	Reset	2.1
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SECTION 4	FAULT-AREA CORRELATION	4.1

FIGURES

3.1 Diagnosing a "Garbage" Fault

SECTION 1

INTRODUCTION

At the most basic level, the LINK 480Z microcomputer consists of one mainboard, a separate switch-mode PSU, and an internal keyboard. An optional add-on board and provision for use as a network station are also available.

This guide is intended to supplement the RML servicing course for a basic LINK 480Z system.

It serves to:

- introduce the 480Z with a brief functional description including block diagram, principles of operation, options, and essential circuit diagrams
- explain the problem of dealing with a non-functioning unit, (i.e. one that is unable to self-diagnose) and methods of introducing diagnostic software via PROMs
- suggest diagnostic routes, flow diagrams, and fault-area correlators
- conclude with experience gained on fault types and symptoms.

SECTION 2

BRIEF CIRCUIT DESCRIPTION

(Circuit : LINK 480Z MAIN BOARD DI0829 SHTS 1-6
LINK 480Z MAIN BOARD MKII DI2093 SHTS 1-7)

PROCESSOR

4MHz Z80A.

One 'wait' state every memory cycle - as in the 380Z - and each VDU access.

RESET

Reset logic pulses reset the processor during power-up and while the RESET button is pressed. Reset is active for 128us and inactive for 512us, and is synchronized with M1 to preserve memory contents during reset. Keyboard reset is automatically activated on power-up, or after reset, and must be cleared during ROS initialization by setting bit 6 on port 1.

SINGLE STEP

Single-step logic is as on the 380Z. An NMI is generated following the eighth M1 cycle after NMIEN goes active 'high'. Note that NMIEN is inactive on power-up, or after reset, so that it need not be de-activated as on the 380Z.

MEMORY

- ROM

  There are sockets for 4 ROM/EPROMs, each of 2 to 8 Kbytes. Mapping of the ROMs is controlled by a PROM (2K resolution) which allows for four entirely independent maps selected by two bits in a port (PAGE 0 and PAGE 1). Map 0 is automatically selected on power-up and reset. For any given map any address space which is not occupied by ROM is occupied by RAM.

- RAM

  RAM mapping is controlled by a writable lookup table. This takes the top two bits of the processor address bus (A15 and A14) and separates four address bits (MA14 - MA17). Of these, MA16 and MA17 select which of the four banks of RAM is to be accessed while the remaining two bits are used to select which of the four 16K pages within a bank of 64K RAM is to be used. This allows any of the sixteen 16K pages to be mapped into any of the four 64K pages of processor address space. The RAM mapping is controlled by writing to port 0 (see later).

- VDU

  The VDU is transparent for both reading and writing (except that one 'wait' state is added to all accesses). The VDU is switchable under software control between 40 and 80 characters. However, the screen contents will be jumbled on changeover and so the screen should be cleared first. The VDU is mapped as I/O ports and should be accessed using:

```
IN  r,C
OUT (C),r
OTI, OTIR, INI, INIR
```

  In all of these cases the value in C will be the Y coordinate of the character on the screen (range 0 to 17H) and the value in B will be the X coordinate (range 0 to 50H). Character 0,0 is at the top left. The value in r will be the character output from reading back the screen. Characters 128 to 191 are dim.

KEYBOARD

The keyboard is of the key-down/key-up variety. This means that when a key is pressed or released the keyboard generates a character. The keyboard will return an 8-bit number of which 6 bits identify the key (a seventh bit is available for future expansion) and 1 bit identifies the direction of travel. The number has no correspondence with ASCII. SHIFT, CTRL, REPEAT, etc. are treated as ordinary keys. The decoding of function keys (including the REPEAT key) is done under software control.

A keyboard 'ready' bit is available in one of the ports and keyboard strobe is connected to channel 2 of the CTC. Characters are read from the keyboard port during interrupt servicing and this clears the ready flag. On power-up, the keyboard reset will go active. Once the CTC (etc.) is set up and it is safe for the keyboard to interrupt, this rail should be taken inactive and the keyboard will then list all the keys currently pressed.

CASSETTE SYSTEM

The input section of the cassette system is identical to that of the 380Z. Thus there is one bit for volume and one bit for data in a port. The data bit is connected to one channel of the CTC so that it can generate an interrupt. (Not used at present.)

On output, the final stages of the frequency generation are performed by the CTC (channel 1). This is fed with 125kHz which can be divided by 26 or 52 to generate 4800Hz or 2400Hz pulses. These are then fed through a divide-by-two stage to generate a 2400Hz or 1200Hz square wave which is filtered and fed to the cassette recorder. For this signal to reach the cassette recorder, the CASWREN bit must be 0. The cassette output bit (after the divide-by-two used to generate an equal mark/space ratio) is readable in a port so that the output phase may be determined.

JOYSTICK INTERFACE

The joystick interface consists of two monostables whose timing resistor consists largely of external potentiometers within the joystick. These monostables can be triggered by a positive edge on JTRIG and their outputs can be read as JT1 and JT2. The monostable time constant is about 1ms centre position. There is also provision for two push buttons which are read through JB1 and JB2.

SERIAL INTERFACES

There is a software 'SIO2' RS232 interface consisting of two bits in an input port (RXD and handshake-CTS) and an output bit (TXD).

There is also a hardware SIO4 RS232 using the Zilog SIO channel B.

PARALLEL PORT (User I/O Port)

Control/Status port 5 is the USERIO port.

There is a hardware handshake provided on the USERIO input port. Data is latched into the port on the positive edge of the strobe line and sets a 'ready' bit which can be ready by the computer, and a 'busy' bit for the peripheral. When the USERIO port is subsequently read by the computer these bits are cleared. Note that the USERIO port is transparent and behaves as in a 380Z if the strobe is held low (by default). In addition to the hardware handshake there is a software handshake (3 output bits, 1 input bit).

CONTROL PORTS

- I/O port map

Device/Port	Address
VDU	0 to 17H
Control/Status port 0	18H
Control/Status port 1	19H
Control/Status port 2	1AH
Control/Status port 3	1BH
Control/Status port 5	1DH
CTC	20 to 23H
SIO	24 to 27H

- Port 0

Read = DIL switches
Write = RAM mapping lookup table

Read	Bit	Write
DIL switch 7	7	x
DIL switch 6	6	x
DIL switch 5	5	x
DIL switch 4	4	x
DIL switch 3	3	MA17
DIL switch 2	2	MA16
DIL switch 1	1	MA15
DIL switch 0	0	MA14

On writing to port 0 the least two significant bits in the B register contain the address within the lookup table to which the data is written.

- Port 1

Read	Bit	Write
Network	7	Network
Network	6	Keyboard Reset
Network	5	Soft UHAND3
Hard USERIO Ready	4	Soft UHAND2
Soft UHAND	3	Soft UHAND1
Keyboard Ready	2	NMIEN
Frame Blank	1	Page 1
Line Blank	0	Page 0

- Port 2

Read	Bit	Write
JB2	7	80/40 Select
JB1	6	ALT CHAR SET
JT1	5	LSPEAK
JT2	4	JTRIG
'SIO2' RXD	3	'SIO2' TXD
'SIO2' HAND	2	CASM2
CAS VOL	1	CASMI
CASS IN	0	CASWREN

- Port 3

Read = Keyboard data
Write = D/A Converter

CTC USAGE:

CHANNEL 0 'SIO4 clock' Input 2MHz

Clocks suitable for all baud rates from 110 to 9600 may be obtained using 2MHz in counter mode, and a 4MHz system clock in timer mode.

CHANNEL 1 Timing Input 125KHz

Provides frequency generation for the cassette system and can be used for general purpose timing.

CHANNEL 2 Keyboard Input keyboard strobe

Generates interrupt on pressing or releasing a key.

CHANNEL 4 Repeat Input Frame Blanking

Generates interrupts for repeat key.

SIO USAGE:

CHANNEL A Network
CHANNEL B 'SIO4' RS232 Port

SECTION 3

DIAGNOSTIC ROUTES

Faults in the 480Z can be broadly categorized as follows:

1. Those faults which allow the processor and ROS to operate, giving access to the Front Panel for diagnostic procedures. These include faults such as SIO port failure, cassette port failure, etc.

   This type of fault is the easier to diagnose yet may still require software routines to be written to test the failing circuit. Programs may be entered using a ROM Pack, the Front Panel or cassette.

2. Faults which do not permit ROS to operate sufficiently to be able to use the Front Panel and/or the cassette interface to enter diagnostic software. Faults include 'garbage' when switching on, no keyboard response, etc.

The 480Z differs substantially from the 380Z in circuit operation and in fault-finding technique because it is designed as a one-board (not modular) system. Therefore, it is essential to understand the operation and deduce the faulty condition from within the faulty system; this is particularly relevant to the second category of faults. The problems encountered at RML with repair of production failures led to the invention of small diagnostic routines, blown into EPROMS, which do not require the operating system or RAM to be functional. They provided RAM, screen, and port testing and also set up diagnostic loops in suspect parts of the circuit. This approach is recommended for fast diagnosis.

A flow diagram for diagnosing a 'garbage' fault is shown in figure 1.

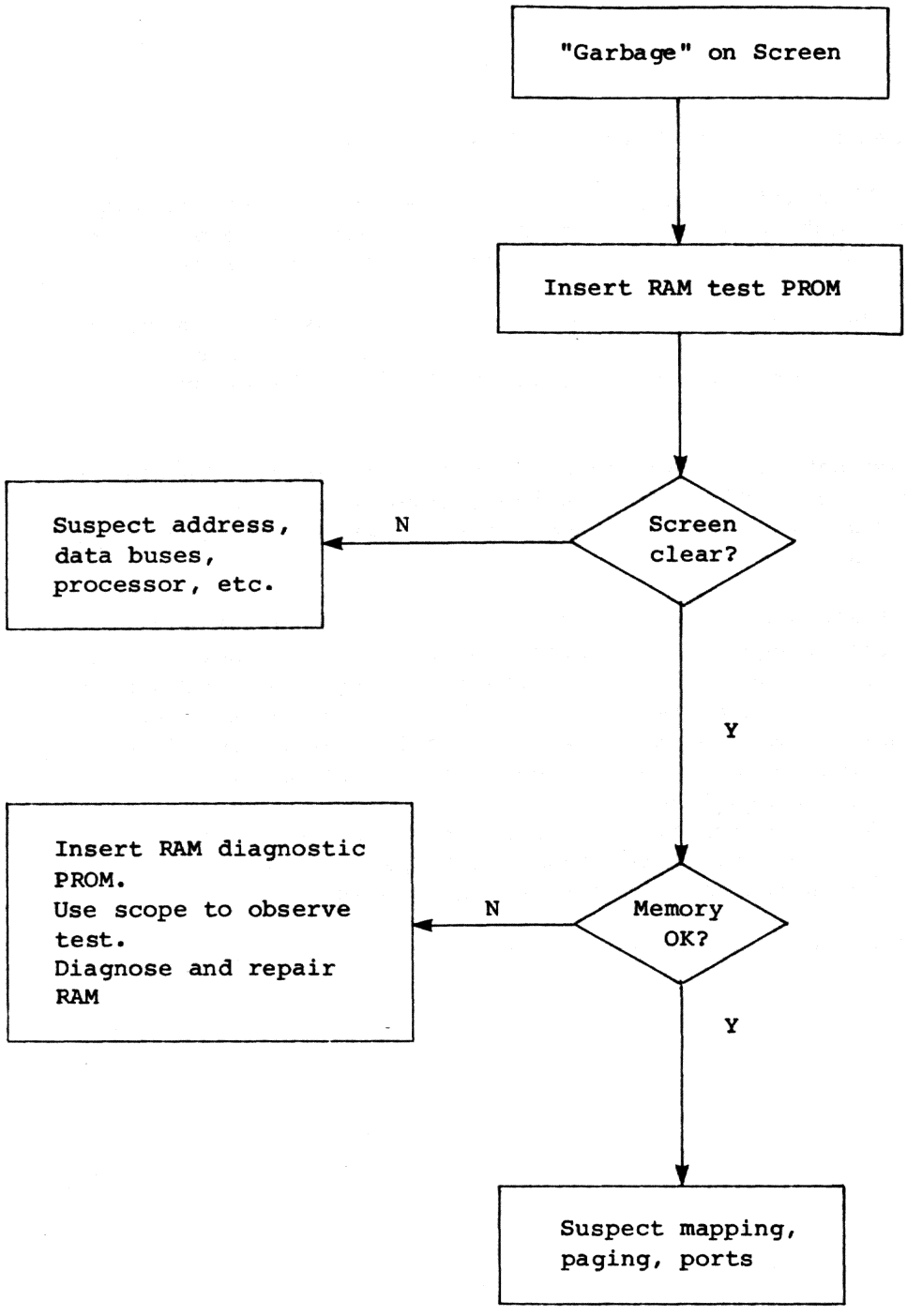


Figure 3.1 Diagnosing a "Garbage" Fault.

SECTION 4

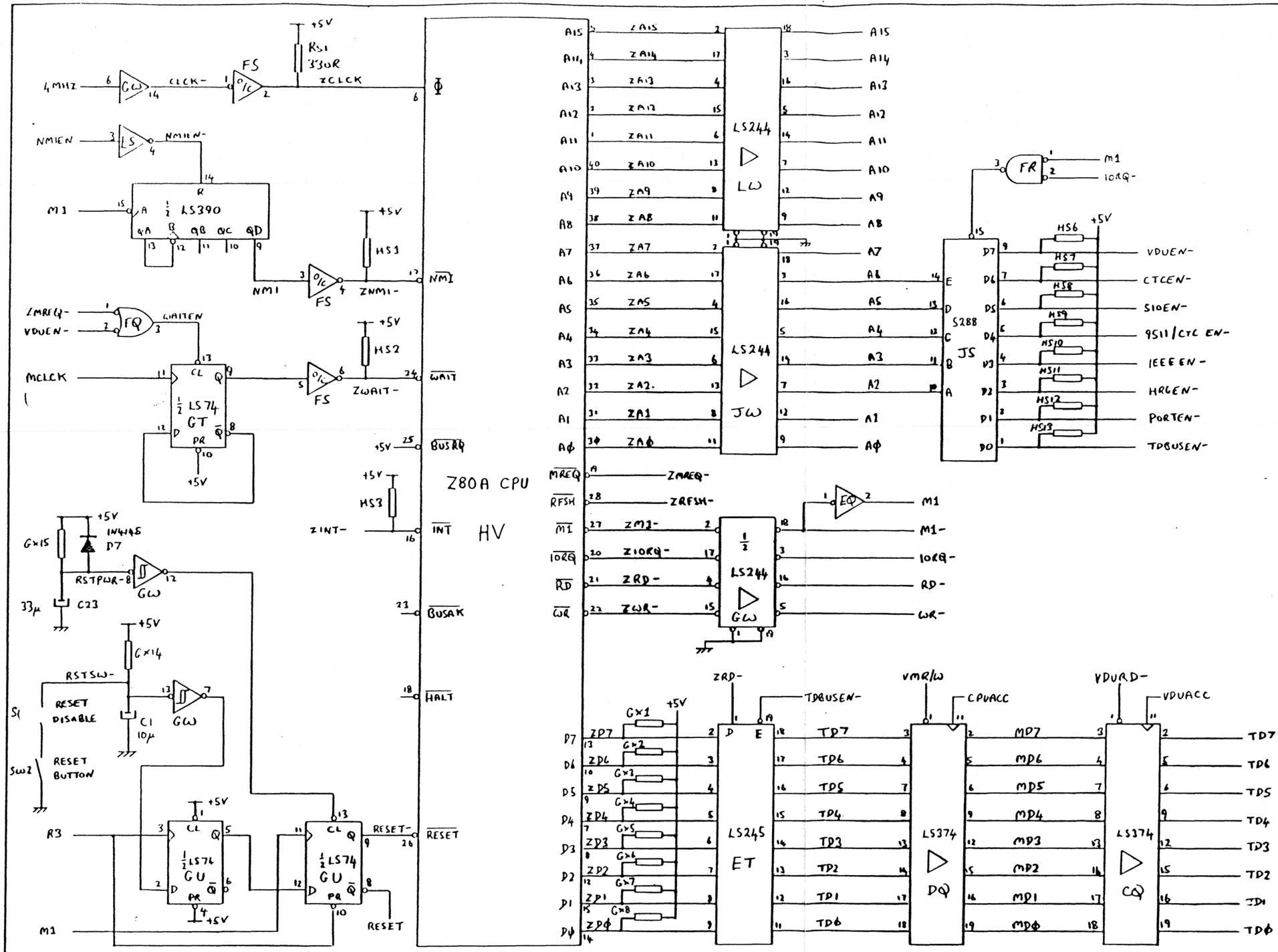
FAULT-AREA CORRELATION

Use this section to identify areas of the circuit likely to be responsible for fault symptoms. Refer to the following table.

Fault Symptom	Suspicious Areas	Diagnostic Procedure
1. No Keyboard Response	Keyboard, CTC, RDPORT3, Memory, Int, ROM	Check KBD ready, ICs BP GW, DP; look for keyboard strobe, processor generally enters for keyboard INT
2. No Cassette Send/Rec	CTC, IC CP, RDPORT2 RAM	Test memory, check signal path for fault
3. No Front Panel	System RAM, System ROM	Test memory
4. Garbage on Power-up	ZDBUS, TDBUS, ZABUS, ABUS, RAM, Mapping, Paging, VDU memory & addressing, processor	Follow flow diagram. Check processor state. Use test PROMs.
5. No display	Clock, PSU, video o/p stages	Check suspicious areas in turn
6. Locks up	Check earthing revision INT, RAM, processor	Check suspicious areas Test memory

CONCLUSION

This supplement makes no attempt to be a comprehensive guide to service on the 480Z. Experience has shown from production servicing that system RAM is fundamental to operation, and almost any symptom can be attributed to faulty system RAM.



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WP 1001

Research Machines Ltd

DATE	DRAWN BY	CHECKED BY
25/8/81	K.F.O.W.	

TITLE

LINK 480Z MAIN BOARD
-PROCESSOR SUPPORT & PORT DECODING

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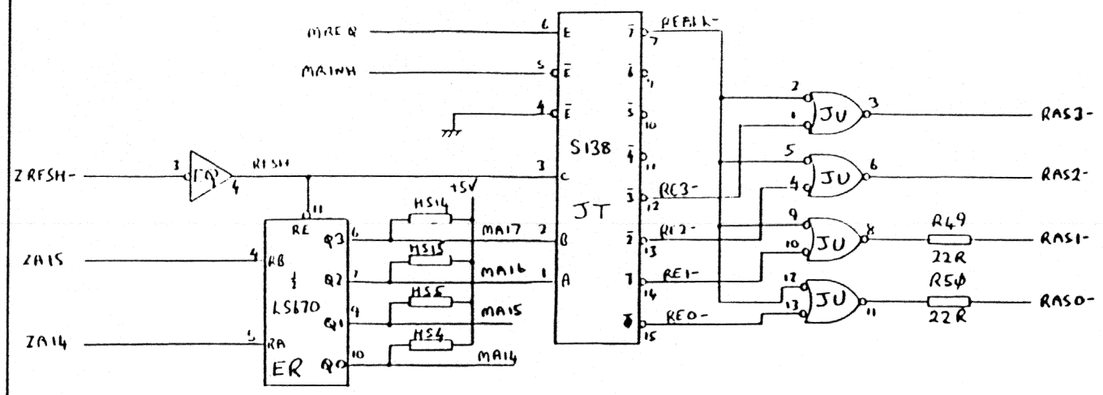

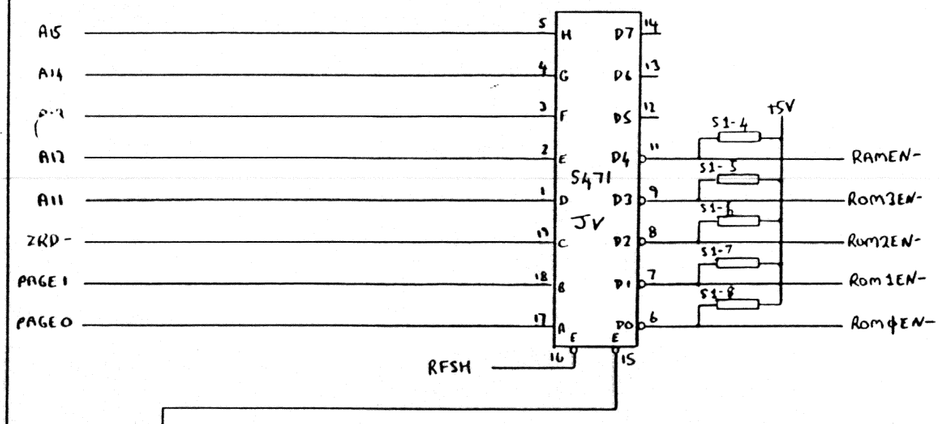

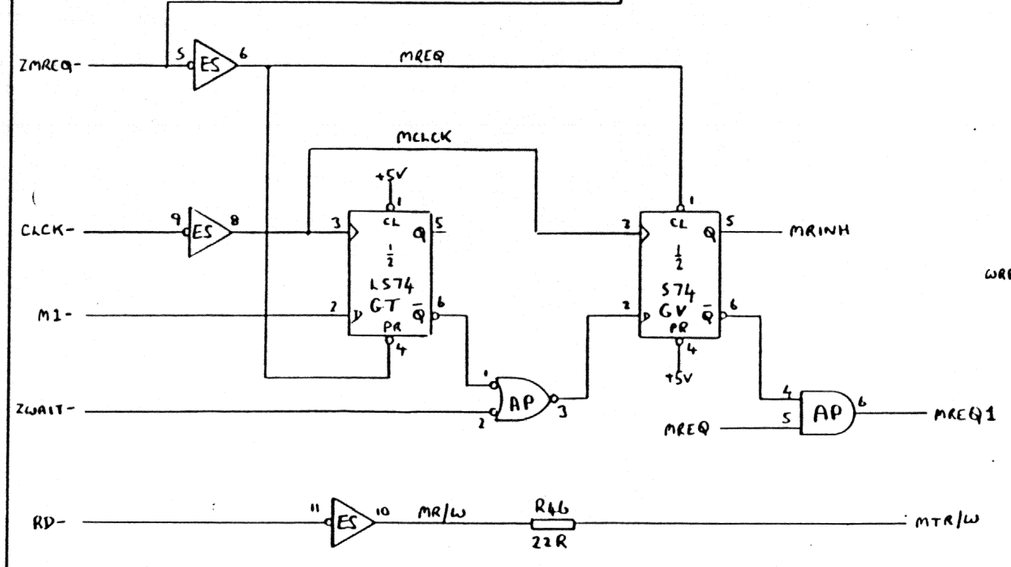

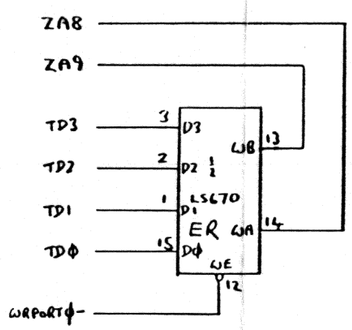

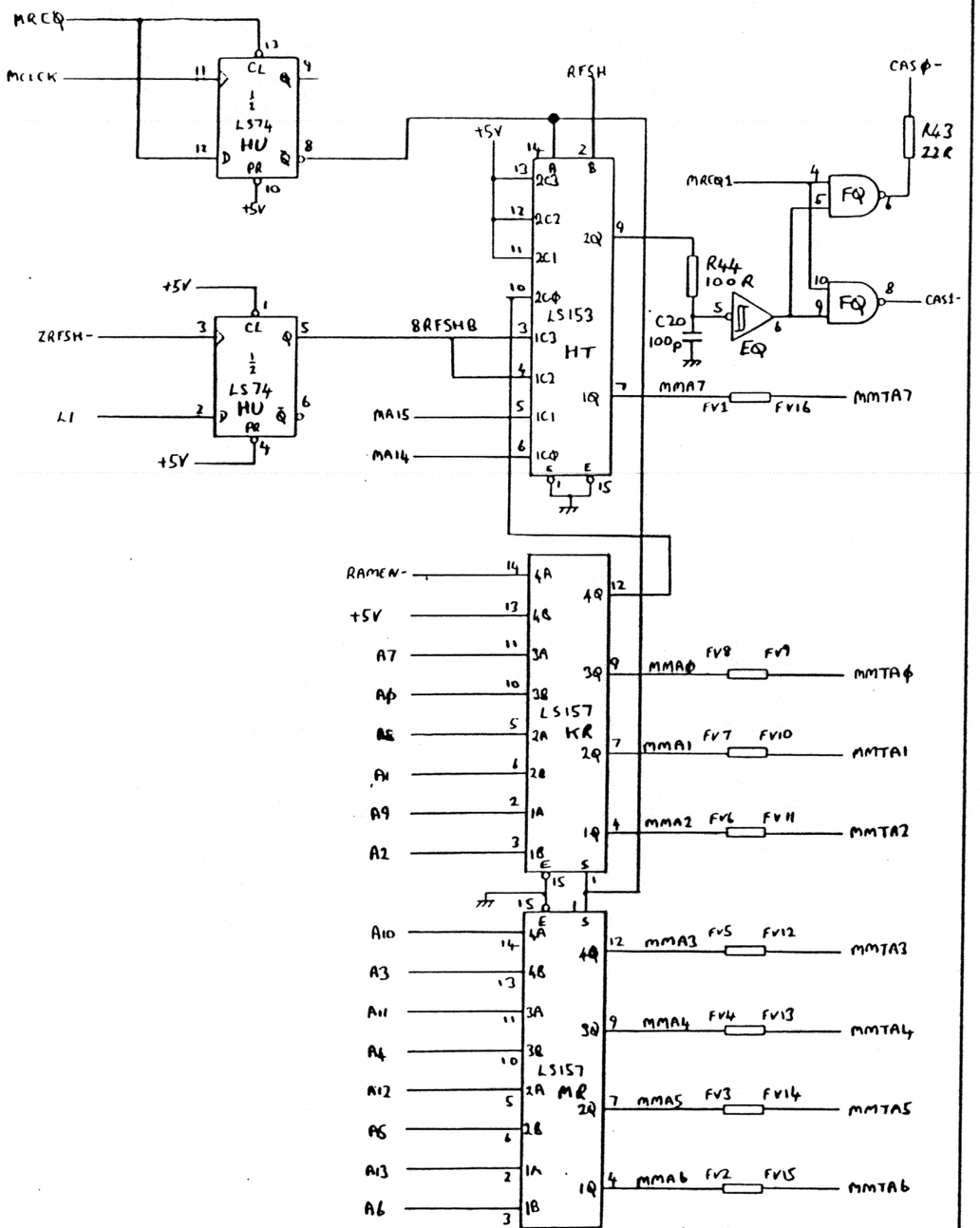

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TITLE

LINK 480Z MAIN BOARD

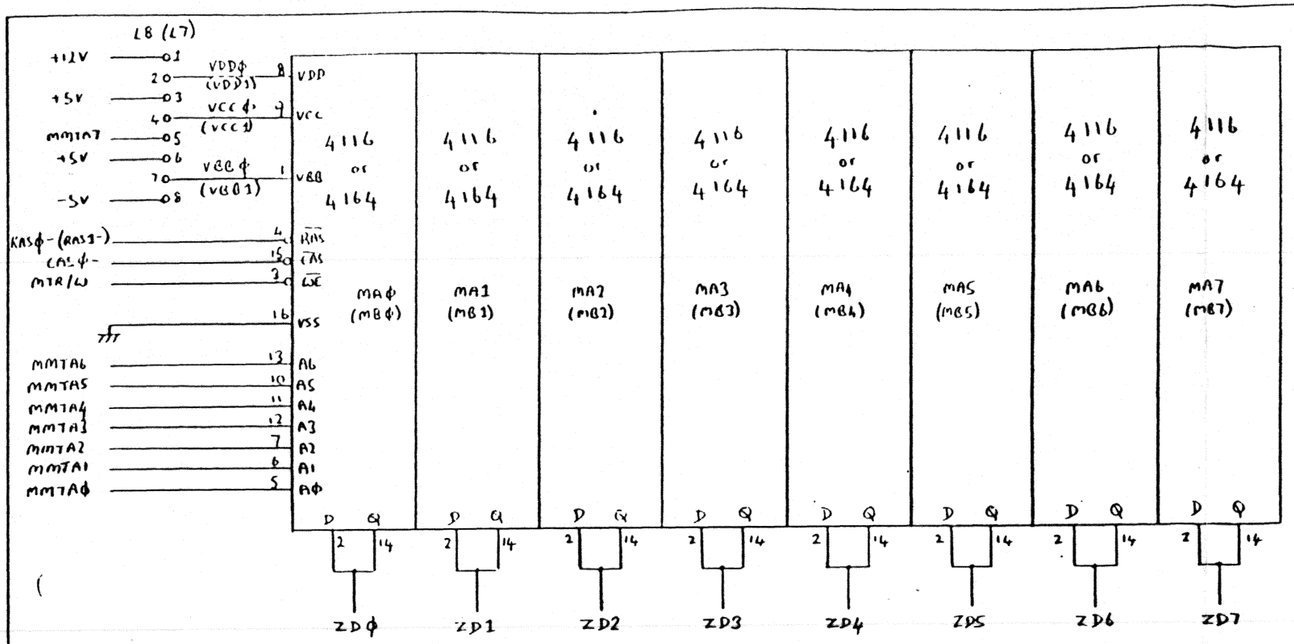
-MEMORY SYSTEM - DECODING/TIMING.

DRAWING NO.

D10829 SHT 2 OF 6

WP 1001

LM2/0



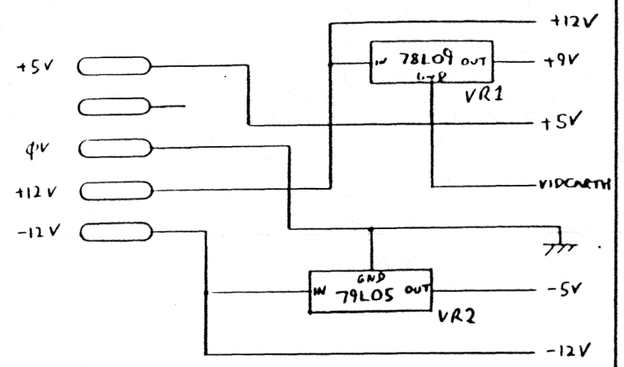
TWO BANKS OF DYNAMIC RAM MAϕ-7 AND MBϕ-7. EACH BANK CAN CONTAIN EITHER 8 × 4116 OR 8 × 4164 THE TYPES OF CHIP INSTALLED IN A PARTICULAR RAM BANK IS SELECTED WITH THE ROW OF LINK PINS ASSOCIATED WITH THAT BANK - L8 FOR BANK ϕ AND L7 FOR BANK 1.

FOR 4116's LINK PINS:-

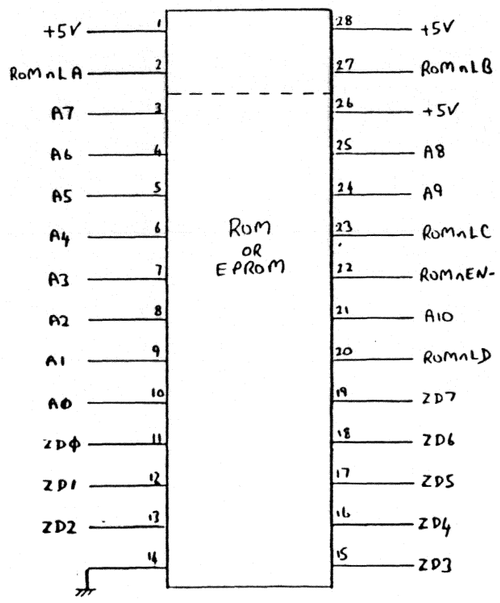
1-2 , 3-4 , 7-8

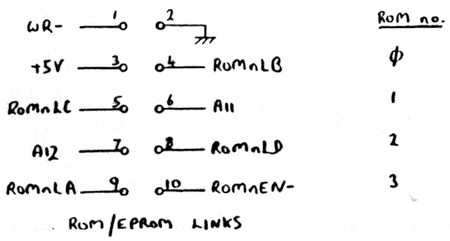
FOR 4164's LINK PINS:-

2-3 , 4-5 , 6-7



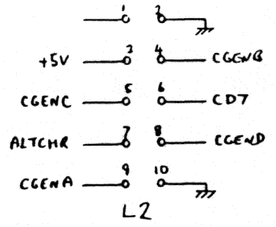
ALL POWER SUPPLY LINES (+12V, +9V, +5V, -5V, -12V) ARE DECOUPLED WITH A MIXTURE OF CERAMIC CAPS (Cw) AND TANTALUM BEADS (Ct FOR 5V, Cu FOR OTHERS) CONNECTED FROM THE SUPPLY TO GROUND (EXCEPT FOR +9V WHICH IS DECOUPLED TO VIDEARTH)

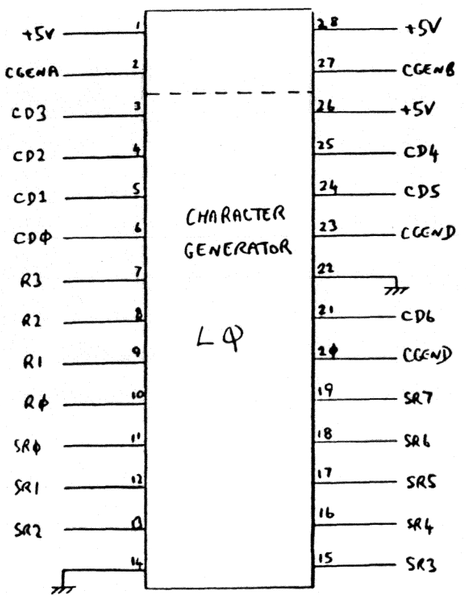




ROM/EPROM LINKS

ROM no.	CHIP	LINKS	n
ϕ	L5	L3	ϕ
1	LT	L4	1
2	LU	L5	2
3	LV	L6	3





THERE ARE 4 SOCKETS FOR ROM; OR EPROM; CONTAINING SYSTEM OR APPLICATION SOFTWARE. EACH OF THESE SOCKETS HAS, ASSOCIATED WITH IT, A SET OF LINK PINS BY SUITABLE CONNECTION OF THESE A LARGE VARIETY OF ROM; OR EPROM; OF THE 5V ONLY VARIETY MAY BE USED, RANGING IN SIZE FROM 2K Bytes to 8K Bytes.

N.B. WHEN INSTALLING 24 PIN DEVICES PINS 3-26 OF THE SOCKET SHOULD BE USED.

AS WITH THE ROM SOCKETS THE CHARACTER GENERATOR SOCKET CAN SUPPORT MOST TYPES OF ROM/EPROM

CHIP	CONNECT LINKS:-
2516/2716	3-5 , 8-10
2532	3-5 , 6-8
2732	5-6 , 8-10
2564	2-4 , 5-7 , 6-8 , 9-10
2764	1-4 , 5-6 , 7-9 , 8-10
68764	5-7 , 6-8

MODIFICATION	Iss	Date	ECN
	1	29-1-82	
	2	10-09-84	

Research Machines Ltd

DATE	DRAWN BY	CHECKED BY
27/8/81	K Ford	

TITLE: LINK 480Z MAIN BOARD
RAM & ROM ARRAYS, CHARACTER GENERATOR & POWER

DRAWING NO. D10829 SHT 3 OF 6

WP 1001

OSC3 X1 - 16.0MHz OSC3 470R R48 470R OSC2 R47 10p C22 JR AQ 16MHZ 16MHZ1 LS161 JP 8MHZ 4MHZ +5V EOC+ EOC- VDUACC CPUACC JR 80/40 LS393 IP LS393 IQ ½ LS390 HR S287 (LINE) GR S287 (FRAME) HQ LS377 FP LS 298 KP VMA0 VMA1 VMA2 VMA3 RD- VDUEN- WR- VDUEN- VDUWR- GS FR FQ LOAD- LBLNK FBLNK EQ DIM2- DIM1- FS FBLNK1 FSYNC1 FR1 LCLK FR LSYNC MSYNC- FSYNC CD7- CD6 DIM2- ES 80/40 40/80 LS 157 GQ LP GP MP LS 298 VMA8 VMA9 VMA10 VMA11 VMR/W VMA4 VMA5 VMA6 VMA7 CCBE LL1 LL2 LL3 LL4 CC3 CC4 CC5 CC6 +5V VDUWR- 6116 KQ LS 377 MQ LS 166 JQ ALTCHR A12 A11 A10 A9 A8 A7 A6 A5 A4 CGEN LOAD- 16MHZ SRNW SR7 SR6 SR5 SR4 SR3 SR2 SR1 SR0 S74 GV EOC+ 40/80 +5V MSYNC- DIM1- VIDEO EP IN4148 D6 SYNC- DIM- WIRE FRAME VIDEO R3 680R ASTEC UM1111E36 MD1 UHF VIDEO VIDEARTH +9V R7 2K7 R3? 2K2 R8 2K2 10K CONNECTED ACROSS - RC&R7 COMPOSITE VIDEO J1-1 75R R4 WIRE FRAME VIDEO J1-6 VIDEO EARTH J1-2 D3 D5 D4 IN4148 VIDMIX2 D2 VIDMIX R6 330R VIDMIX1 D1 IN4148 BSX 20 Tr1 R5 1K0 R2 3K9 R1 2R2 -5V AUDIO AUDIO OUT J1-5 R32 2K2 LSYNC LINE SYNC J1-4 FSYNC FRAME SYNC J1-3 80/40 CΦ CC6 LS 157 HP CΦ6 CCBE

MODIFICATION			
Iss	Date	ECN	
A	KAF 2/10/81		
1	29-1-82		
2	10-02-82		

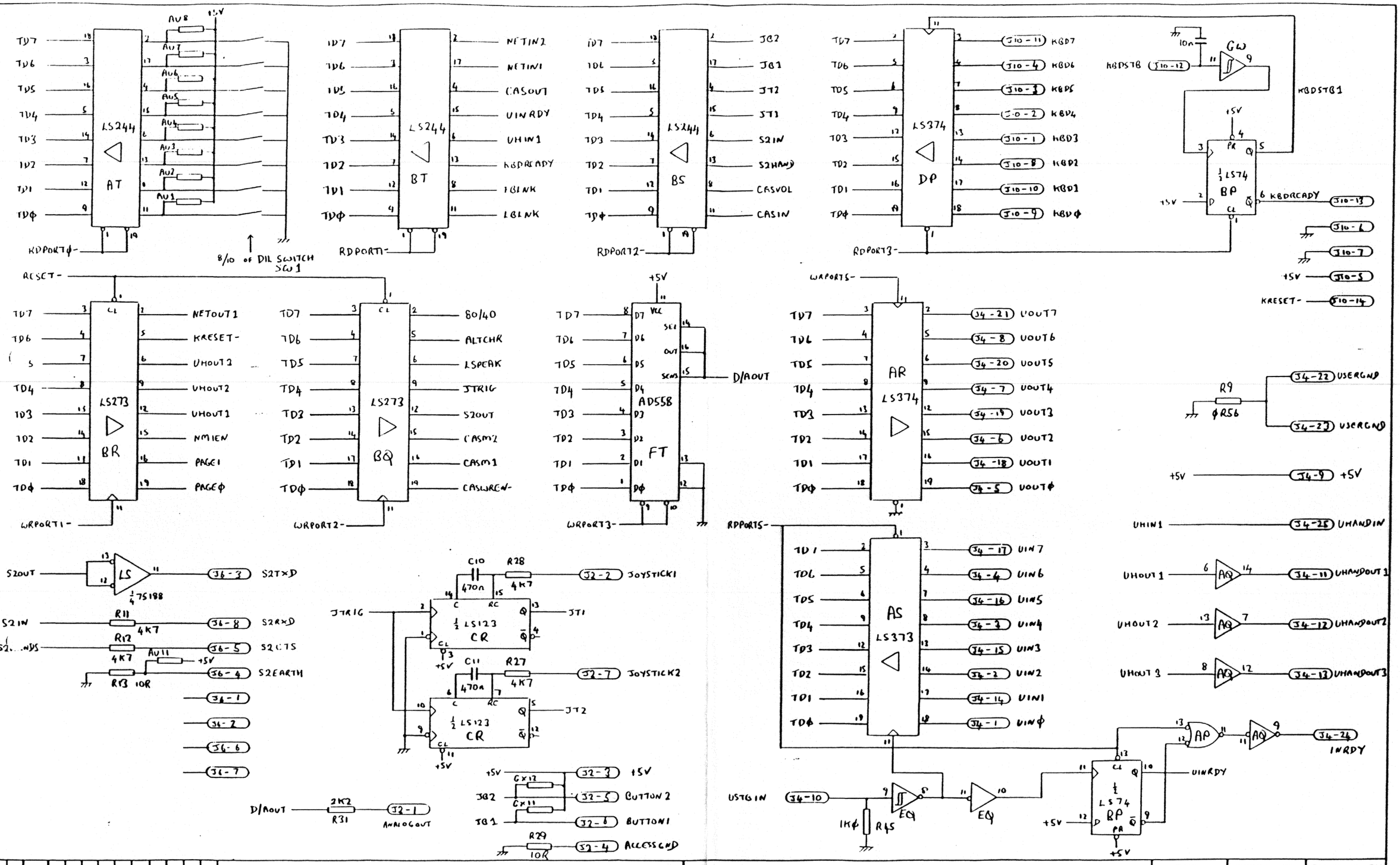
Research Machines Ltd

DATE	DRAWN BY	CHECKED BY
21/8/81	K. Ford	

TITLE: LINK 480Z MAIN BOARD - VDU CIRCUITRY

DRAWING NO. D10829 SHT 4 OF 6

WP1001



MODIFICATION			
A	KAF 26/10/82	Date	ECN
Iss	1	29-1-82	10-03-82

Research Machines Ltd	DATE	DRAWN BY	CHECKED BY
	26/8/8	K. Ford	

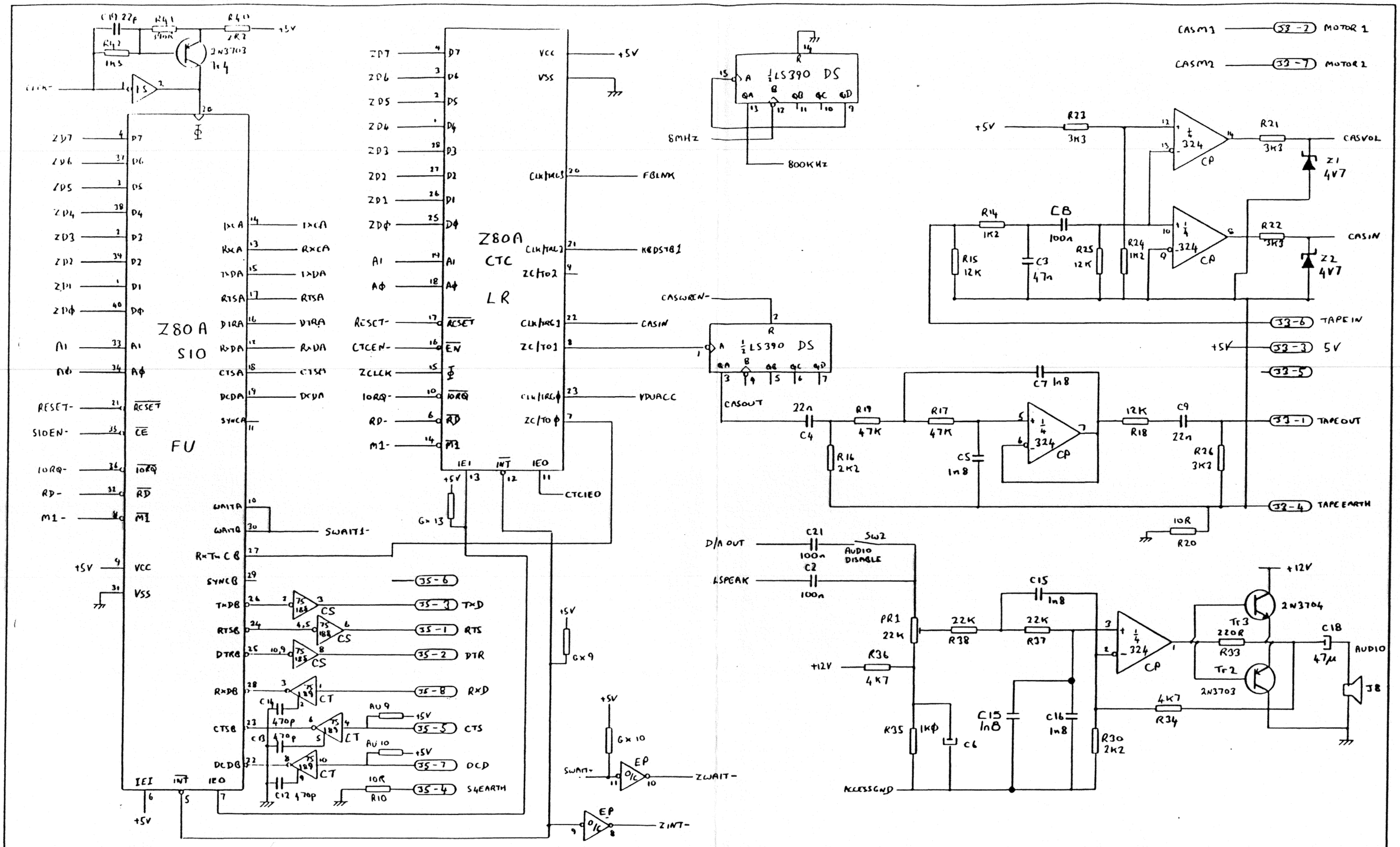
TITLE

LINK 480Z MAIN BOARD

TTL I/O PORTS-KEYBOARD, USER I/O, ACCESSORIES, SIO-2

DRAWING NO. D10829 SHT 5 OF 6

WP 1001



MODIFICATION			ECN
A	KAF 26/10/81		
Iss	Date		
1	29-1-82		
—	10-3-84		

Research Machines Ltd

DATE	DRAWN BY	CHECKED BY
27/8/81	K. Ford	

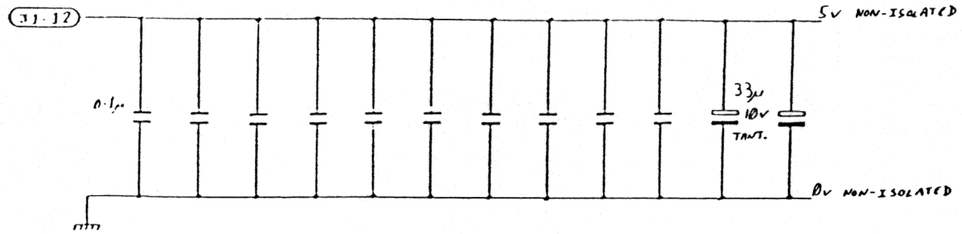
TITLE

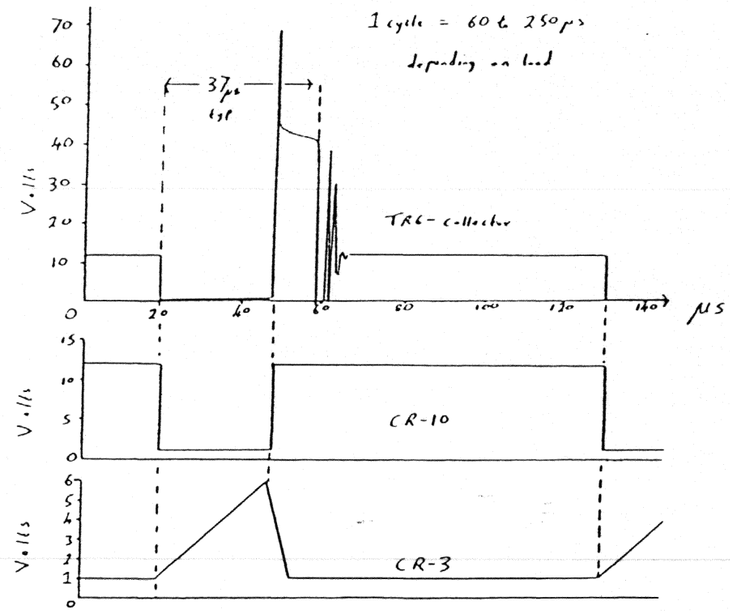
LINK 480Z MAIN BOARD

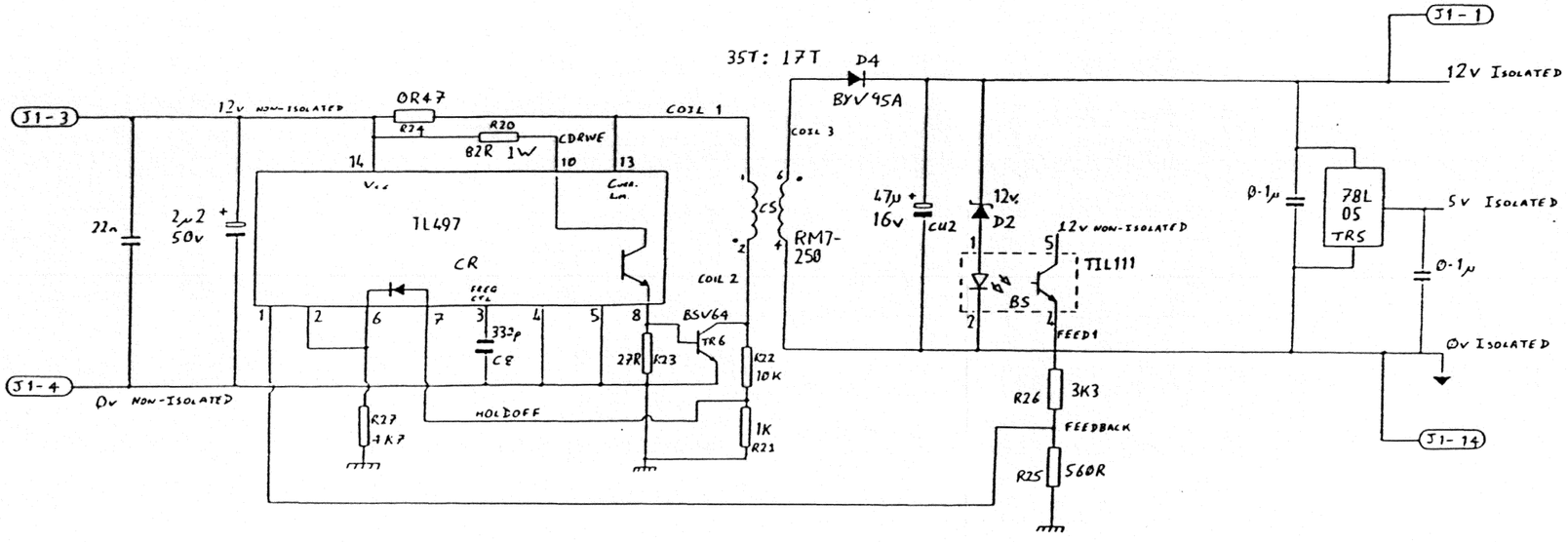
SIO, CTC & ANALOGUE - SIO/4, CASSETTE & AUDIO.

DRAWING NO. D10829 SHT 6 OF 6

WP 1001







MODIFICATION		
A	13/1/82	
B	27/1/82	
C	6/4/82	
D	12/5/82	
E	9/8/82	
F	13/11/12	
G	9/3/84	

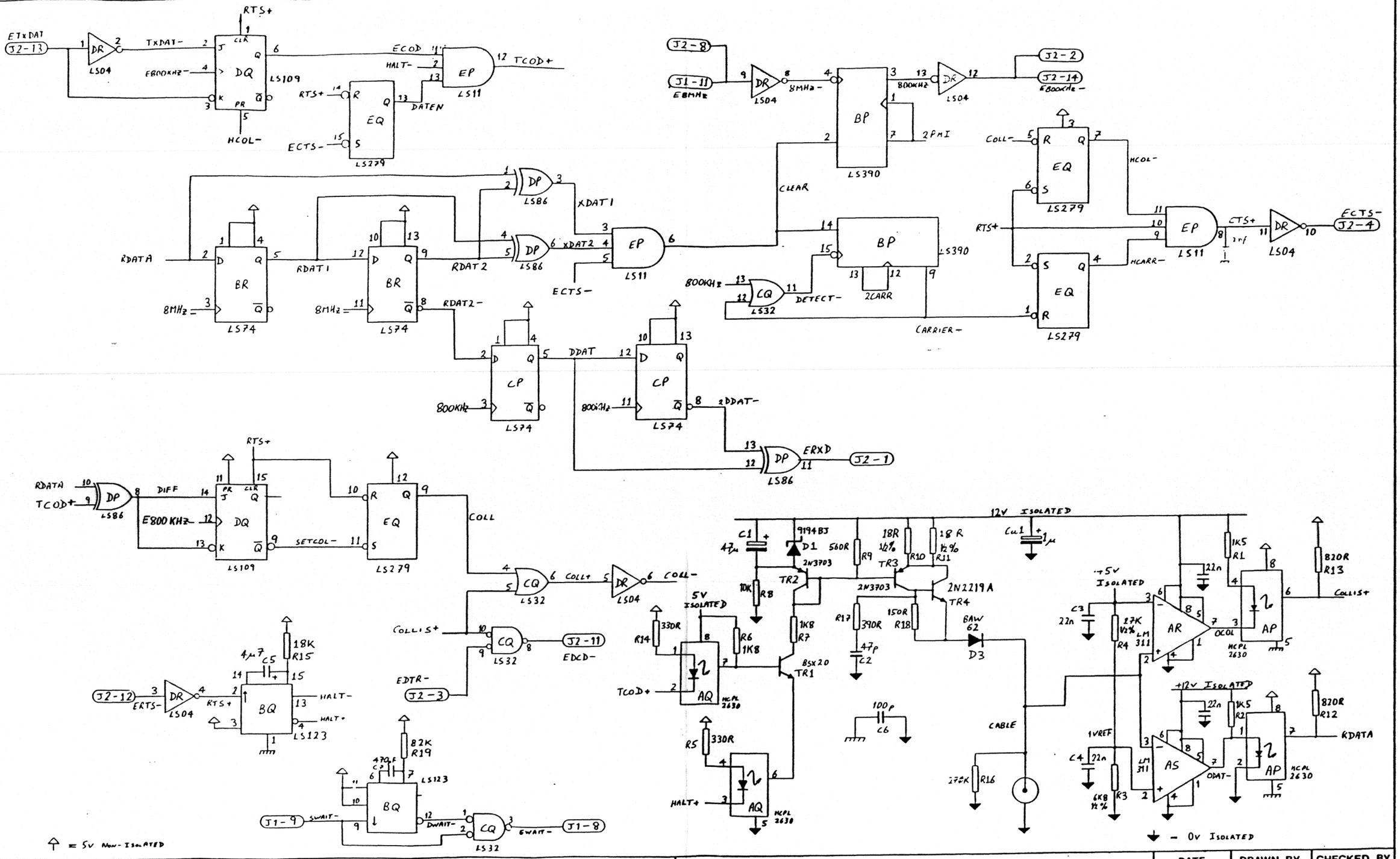
WP 1001

Research Machines Ltd

DATE	DRAWN BY	CHECKED BY
10-12-81	Garth M Davies	

TITLE: TRANSCEIVER POWER SUPPLY ISOLATION

DRAWING NO. 12681 SHT 1 of 2



MODIFICATION		
A	18/11/81	
B	21/11/81	
C	8/11/82	
D	13/1/82	
E	28/1/82	
F	8/2/82	
G	6/4/82	
H	7/5/82	
I	12/5/82	
J	13/5/82	
K	9/8/82	
	19/3/84	

Research Machines Ltd

DATE	DRAWN BY	CHECKED BY
19/10/81		

TITLE: LINK 480Z TRANSCEIVER

DRAWING NO. 12681 sht 2of2

WF 001

Z80A CPU

IC69

R34 330R

IC38 IC50 IC43 IC55 LS390 IC39 IC51 LS74 IC42 LS74 IC38 IC38

4MHZ CLCK- ZCLCK NMIEN NMIEN- M1 NM1 ZNMI- MREQ WAITEN VDUEN- MCLCK ZMREQ- ZWAIT- RSTPWR-B RSTSW- RESET DISABLE RESET BUTTON R3 RESET- RESET M1

1N4148 D8 C60 33µ C59 10µ

RNB RN4 J11 J12

Φ /NMI /WAIT /BUSRQ /INT /BUSAK /HALT /RESET

ZINT-

LS244 IC78 LS244 IC59 LS244 IC38 LS245 IC25 LS374 IC26 LS374 IC32

A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 AΦ

ZA15 ZA14 ZA13 ZA12 ZA11 ZA10 ZA9 ZA8 ZA7 ZA6 ZA5 ZA4 ZA3 ZA2 ZA1 ZAΦ

MREQ RFSH M1 IORQ RD WR

ZMREQ- ZRFSH- ZM1- ZIORQ- ZRD- ZWR-

ZRD- TDBUSEN- VMR/W CPUACC VDURD- VDUACC

ZD7 ZD6 ZD5 ZD4 ZD3 ZD2 ZD1 ZDΦ

TD7 TD6 TD5 TD4 TD3 TD2 TD1 TDΦ

MD7 MD6 MD5 MD4 MD3 MD2 MD1 MDΦ

IC52 M1 IORQ-

S288 IC70 VDUEN- CTCEN- SIOEN- SIO1/CTC EN- IEEEEN- HRGEN- PORTEN- TDBUSEN-

IC10 M1 M1- IORQ- RD- WR-

LS138 IC18 PORTEN- RD- +5V A2 A1 A0 RDPORTS- RDPORT3- RDPORT2- RDPORT1- RDPORTΦ-

LS138 IC19 PORTEN- WR- +5V A2 A1 A0 WRPORTS- WRPORT3- WRPORT2- WRPORT1- WRPORTΦ-

Components	on this	sheet
IC10	R34	C 59
IC18	RN4	C 60
IC19	RNB	
IC25		
IC26		
IC32		
IC38		
IC39	DB	
IC42		
IC43		
IC50	SW1	
IC51	SW2	
IC52		
IC65	J11	
IC69	J12	
IC70		
IC78		

MODIFICATION	ECN	Date	Iss
A 2.6.84		8-9-83	A
		30-9-83	B
		29-2-84	C
	18	15-03-84	1

Research Machines Ltd

DATE	DRAWN BY	CHECKED BY
8-9-83	C A S	D S D

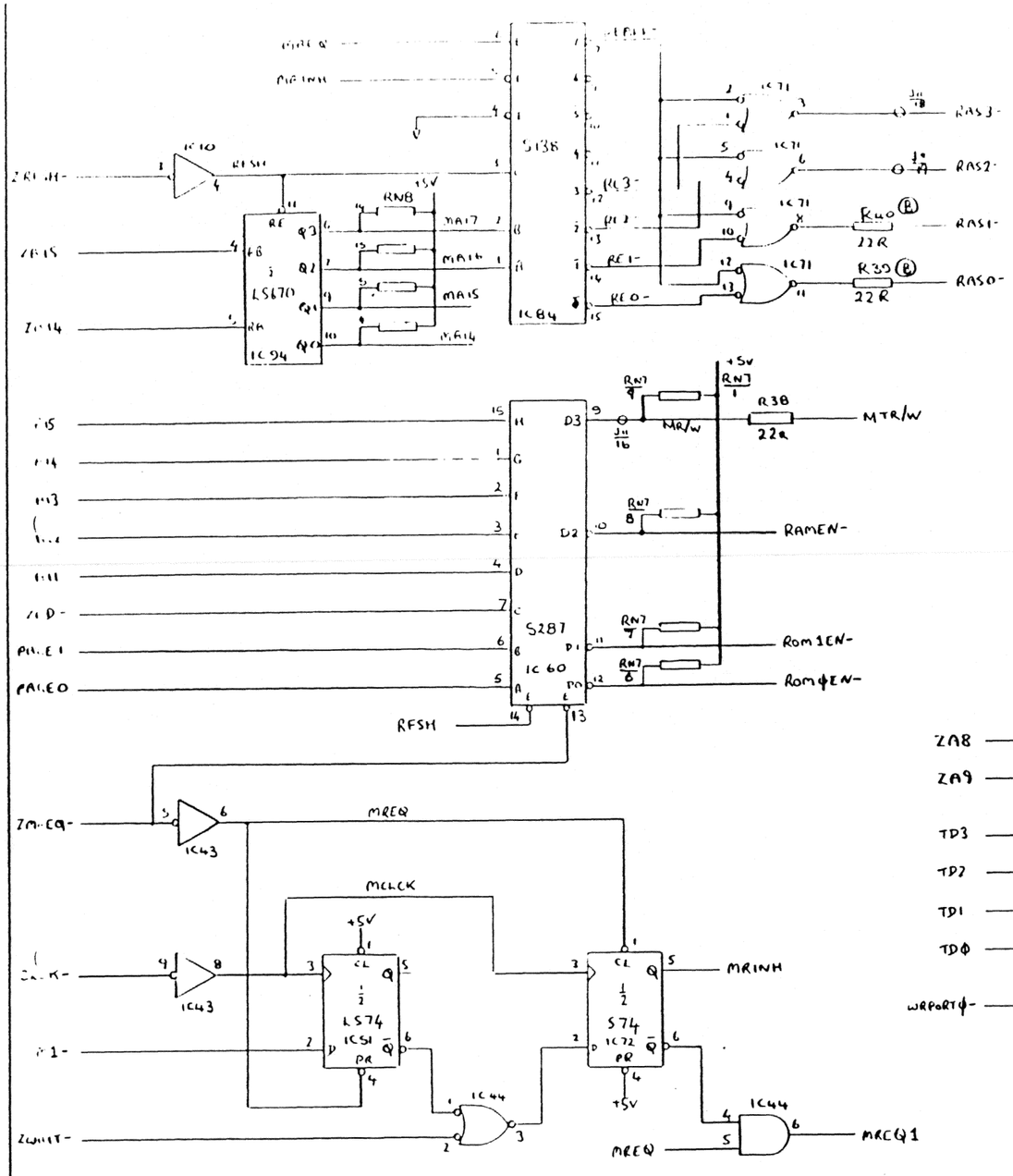
TITLE

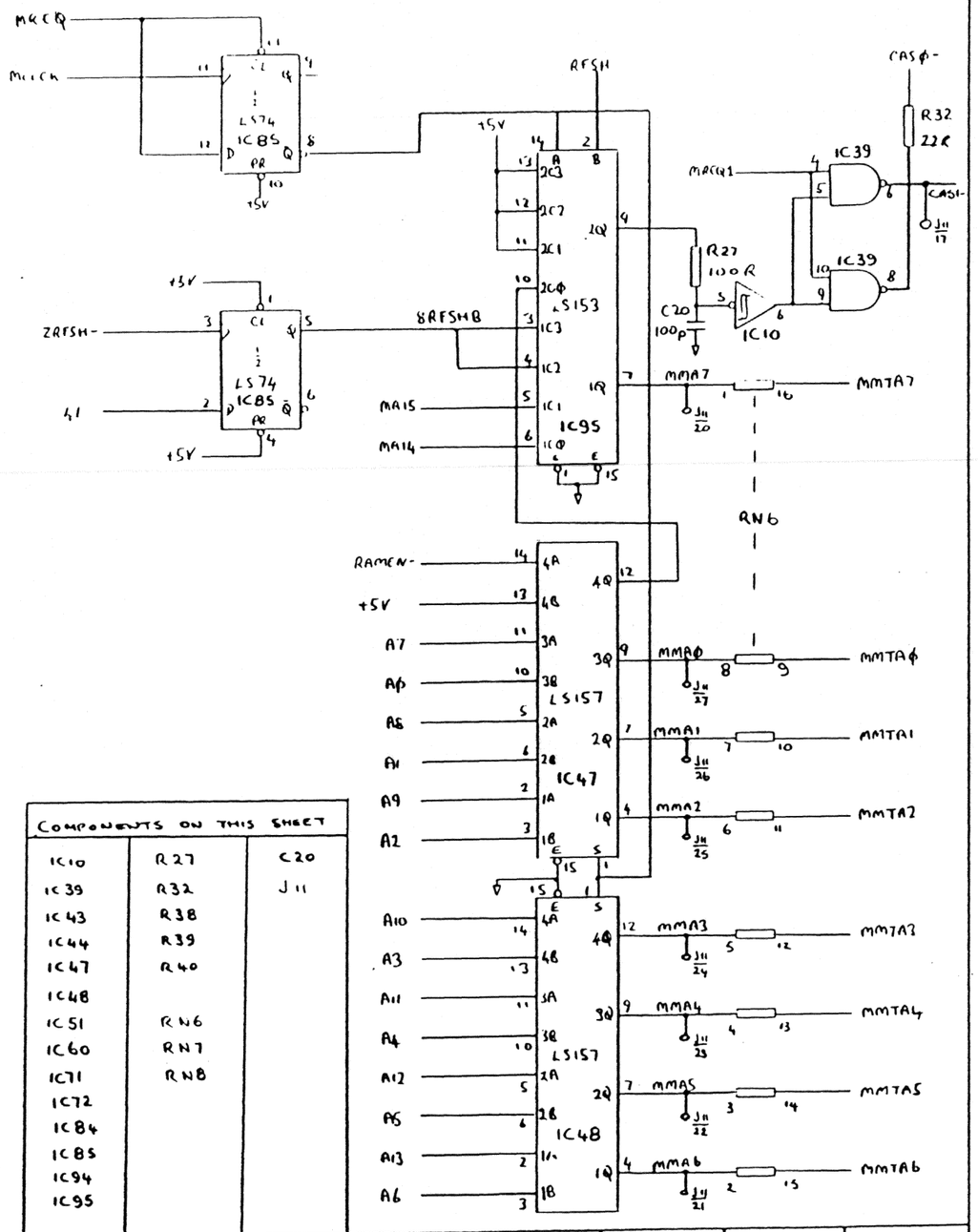
LINK 480Z MAIN BOARD MK 2

-PROCESSOR SUPPORT & PORT DECODING

DRAWING NO. D12053

SHT 1 OF 7





COMPONENTS ON THIS SHEET		
IC10	R27	C20
IC39	R32	J11
IC43	R38	
IC44	R39	
IC47	R40	
IC48		
IC51	RN6	
IC60	RN7	
IC71	RN8	
IC72		
IC84		
IC85		
IC94		
IC95		

MODIFICATION	Iss	Date	ECN
	A	8-9-83	
	B	30-9-83	
	C	29-2-84	
	1	15-05-84	182

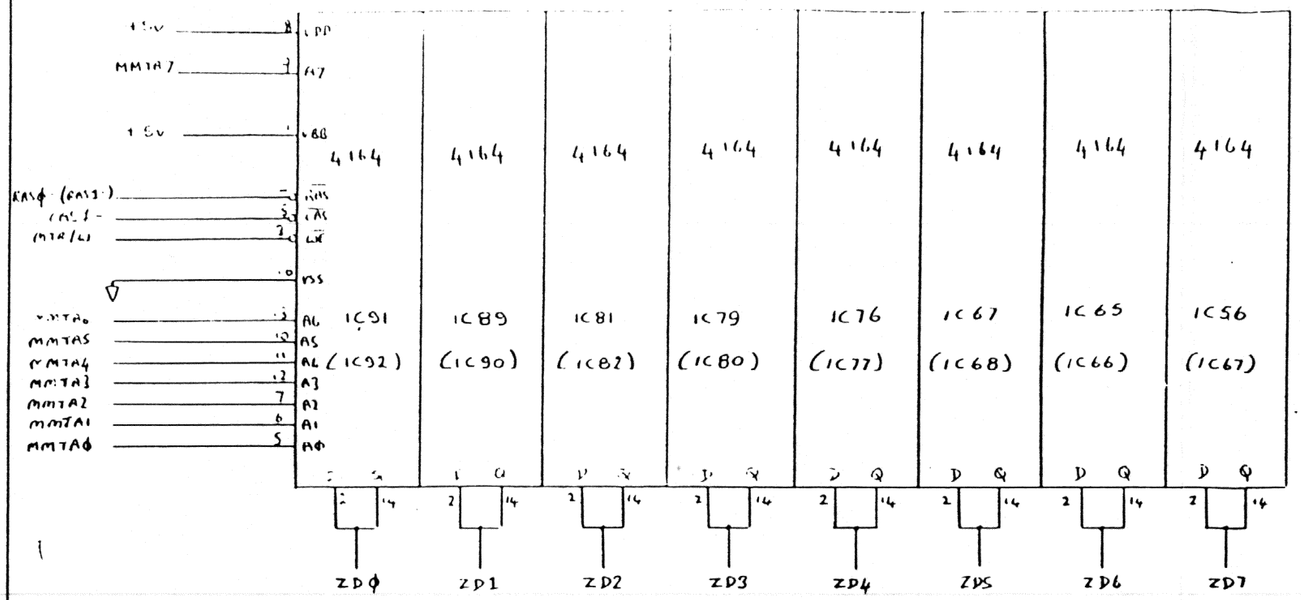
Research Machines Ltd

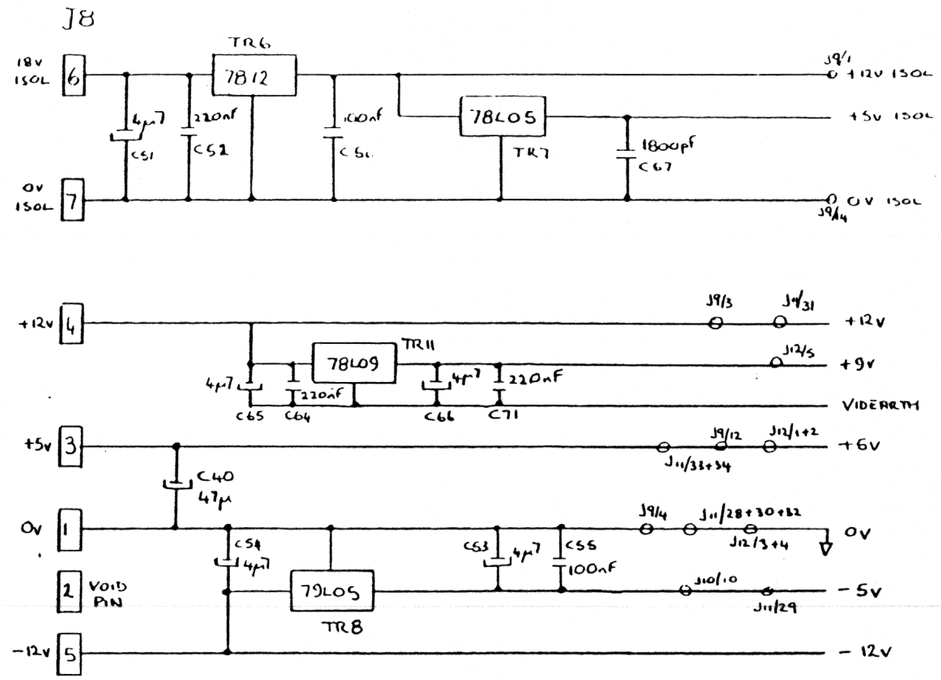
DATE	DRAWN BY	CHECKED BY
8-9-83	C.A.S.	D.S.D

TITLE: LINK 480Z MAIN BOARD MK2
-MEMORY SYSTEM - DECODING/TIMING.

DRAWING NO. D12093

SHT 2 OF 7





COMPONENTS ON THIS SHEET	
IC56	TR6
IC57	TR7
IC65	TR8
IC66 *	TR11
IC67 *	
IC68 *	C51
IC76	C52
IC77 *	C53
IC79	C54
IC80 *	C55
IC81	C56
IC82 *	C57
IC83	C64
IC89	C65
IC90 *	C66
IC91	C71
IC92 *	
IC93	J8 J9 J10
IC98	J11 J12

I.C's MARKED * ARE OPTIONAL MEMORY UPGRADE

MODIFICATION		ECN	Date	Iss
	A		9-9-83	A
	B		30-9-83	B
	C		29-2-84	C
		BR	15-03-84	-

Research Machines Ltd

DATE	DRAWN BY	CHECKED BY
9-9-83	C.A.S	DSD

TITLE: LINK 480Z MAIN BOARD MK 2
RAM & ROM ARRAYS, CHARACTER GENERATOR & POWER

DRAWING NO. D12093 SHT 3 OF 7

COMPONENTS ON THIS SHEET

IC 10	IC 75	R1
IC 36	IC 86	
IC 39	IC 87	J7 J9
IC 40	IC 88	J10 J12
IC 41	IC 96	MD1
IC 43	IC 97	
IC 44	IC 98	TR4
IC 45		
IC 46		D3
IC 52	R 24	D4
IC 53	R 33	D5
IC 54	R 41	D6
IC 55	R 42	D7
IC 61		D11
IC 62	RN2	
IC 63	RN5	
IC 64		
IC 72		
IC 73		
IC 74		

MODIFICATION			ECN
A	KAF 26/10/81		
Iss	Date		
A	8-9-83		
B	20-9-83		
C	25-2-84		182
1	15-03-84		

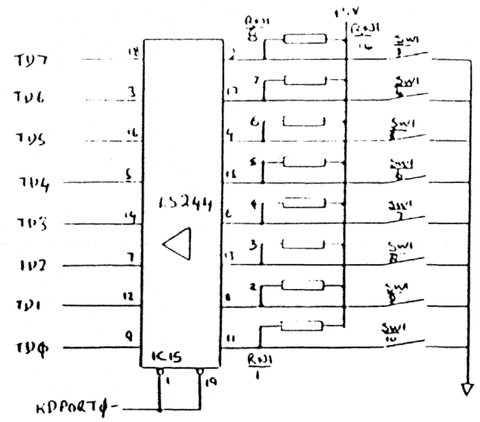
Research Machines Ltd

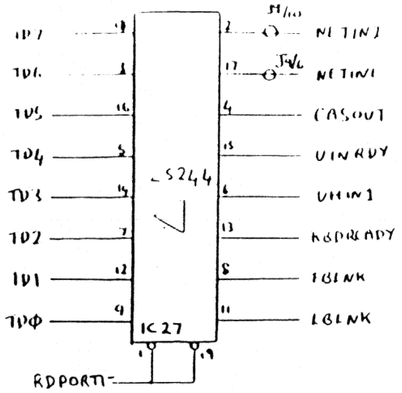
DATE	DRAWN BY	CHECKED BY
8-9-83	C.A.S	DSD

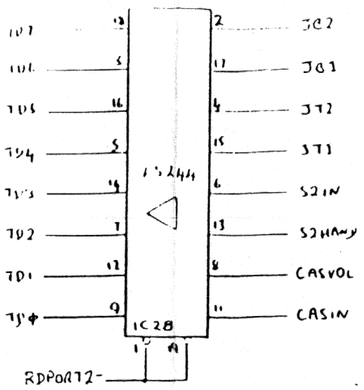
TITLE: LINK 480Z MAIN BOARD MK 2 - VDU CIRCUITRY

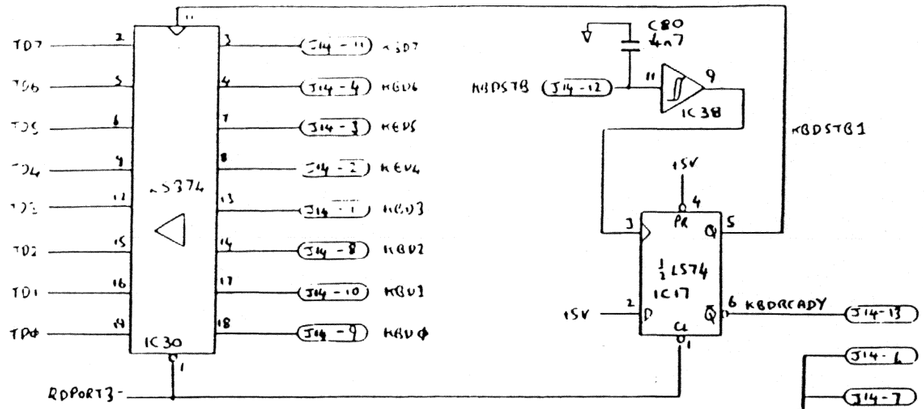
DRAWING NO. D12093 SHT 4 OF 7

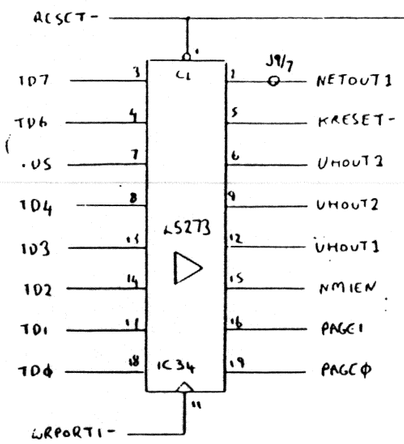
WP 1001

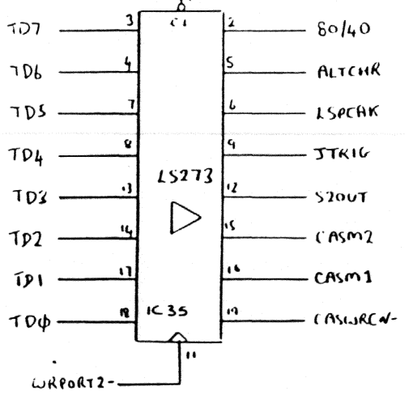


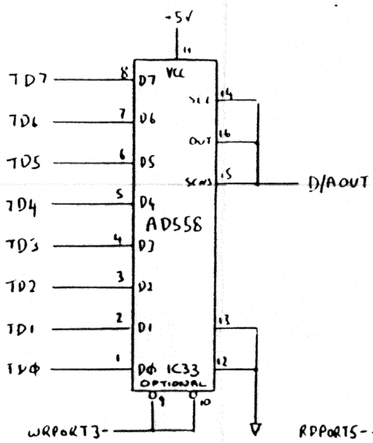


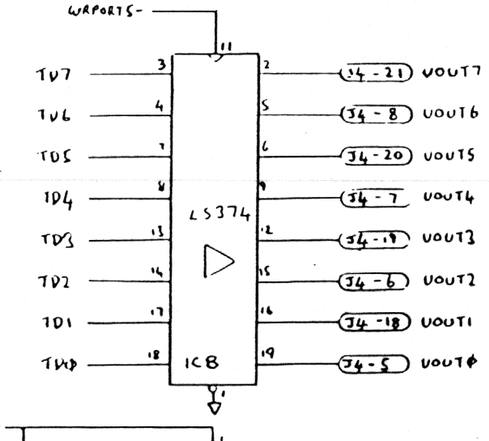


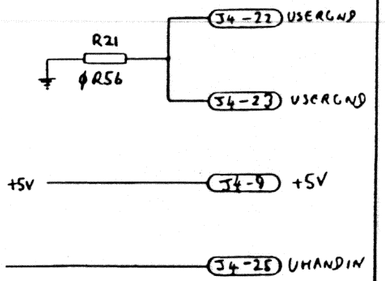


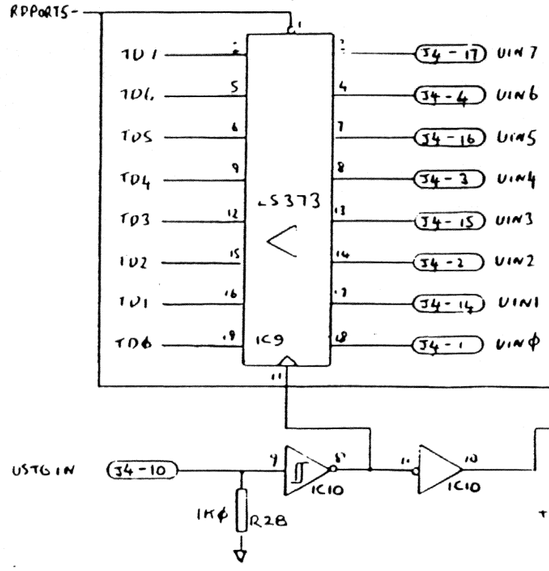


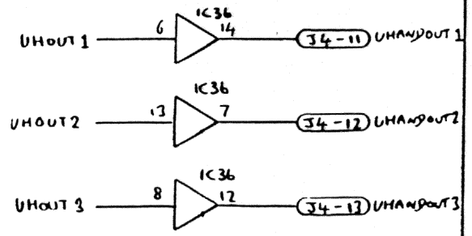


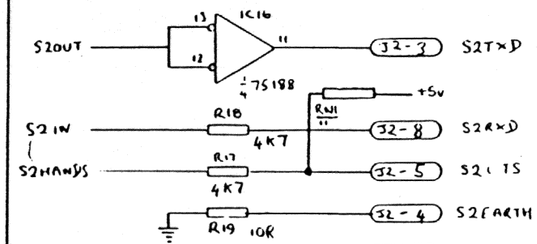


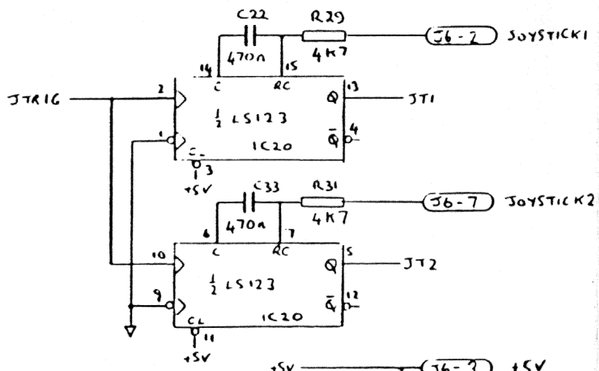












COMPONENTS ON THIS SHEET			
IC8	IC35	R31	J2
IC9	IC36	RN1	J4
IC10	IC38	RN4	J6
IC15	IC44	RN5	J14
IC16			J9
IC17	R17	C22	
IC20	R18	C33	
IC27	R19	C80	
IC28	R21		
IC30	R23	SW1	
IC33	R28		
IC34	R29		

MODIFICATION	Iss	Date	ECN
KAS 2K1 to K2	A	9-9-83	
	B	30-9-83	
	C	29-2-84	182
	1	15-03-84	182

Research Machines Ltd

DATE	DRAWN BY	CHECKED BY
9-9-83	C.A.S	DSD

TITLE: LINK 480Z MAIN BOARD MK2

TTL I/O PORTS-KEYBOARD, USER I/O, ACCESSORIES, SIO-2

DRAWING NO. D12093

SHT 5 OF 7

Z80A SIO
IC49
Z80A CTC
IC58
IC43
IC29
IC21
IC16
IC7
IC46
JN3703 TR12
2N3704 TR9
2N3703 TR10
SIO/1
SIO/2
SIO/3
SIO/4
CTC/125
J3/5
J13/26
J12/26
J13/1
J13/2
J3 - 1 RTS
J3 - 2 DTR
J3 - 3 TXD
J3 - 4 S4EARTH
J3 - 5 CTS
J3 - 6
J3 - 7 DCD
J3 - 8 RXD
55 - 2 MOTOR 1
35 - 7 MOTOR 2
35 - 6 TAPE IN
35 - 3 5V
35 - 5
35 - 1 TAPE OUT
35 - 4 TAPE EARTH
J13-1 AUDIO
J13-2
D10 5v1
D9 5v1
+5V
+12V
6MHz
800KHz
FBLNK
HRDSTB1
CASIN
VDUACC
CTCIEO
SWAIT1-
ZWAIT-
CASMEN-
CASOUT
CASVOL
CASIN
D/A OUT
LSPEAK
AUDIO DISABLE
ACCESSGND
VR1 22K
1KΦ
C49 33μ
C47 47n
C48 1n8
C50 1n8
C36 1n8
C69 1n8
C70 1n8
C72 47μ
C135 100n
C46 100n
C38 100n
C34 22n
C35 22n
C15 470p
C16 470p
C18 470p
R20 10R
R22 10R
SW1 2
RN1 10K
RN2 10K
RN3 1K2
RN4 9 10K
RN5 1 22K
RN5 2 22K
RN5 3 1KΦ
RN5 4 4K7
RN5 5 220R
RN5 11 4K7
RN5 12 2K2
RN5 13 4K7
RN5 14 22K
RN3 1 12K
RN3 2 47K
RN3 3 47K
RN3 4 12K
RN3 5 1K2
RN3 6 3K3
RN3 7 12K
RN3 8 3K3
RN3 9 3K3
RN3 10 3K3
RN3 11 3K3
RN3 12 12K
RN3 13 2K2
RN3 14 12K
RN3 15 10K
RN3 16 10K
RN3 18 47K
RN3 19 1K2
RN3 20 1K2
RN3 21 12K
RN3 22 12K
RN3 23 1K2
RN3 24 12K
RN3 25 1K2
RN3 26 1K2
RN3 27 1K2
RN3 28 1K2
RN3 29 1K2
RN3 30 1K2
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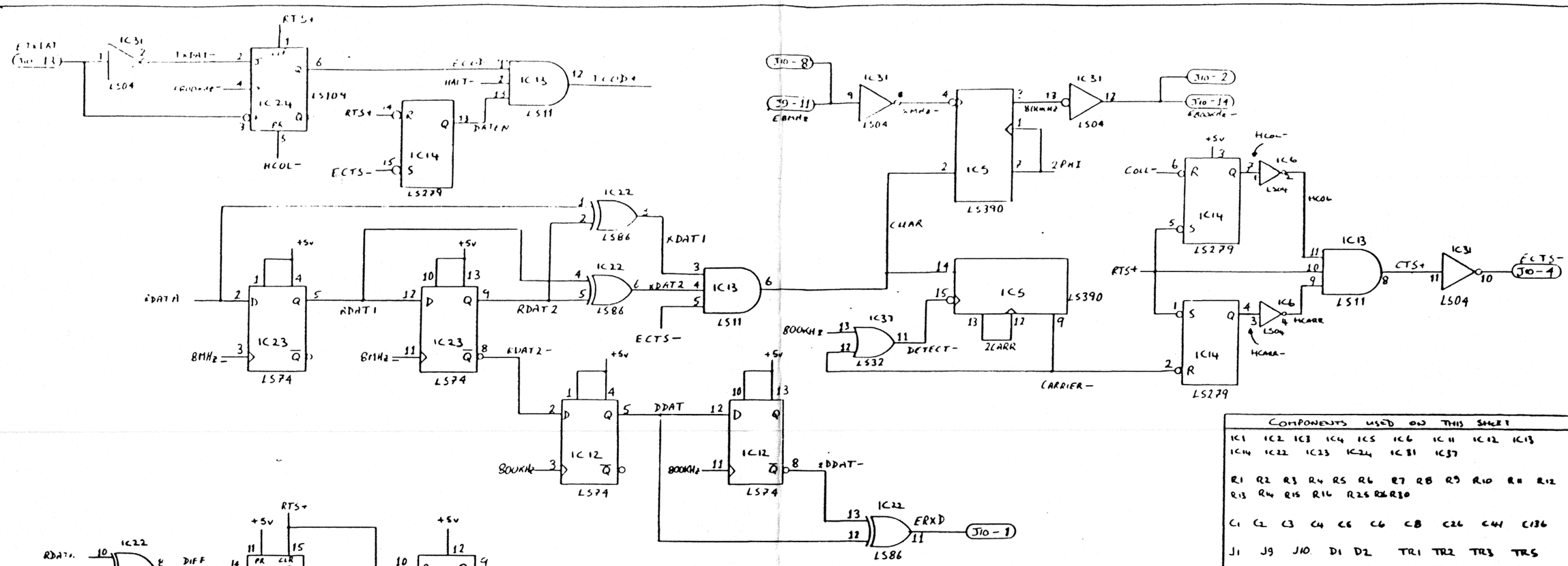
RN3 34 1K2
RN3 35 1K2
RN3 36 1K2
RN3 37 1K2
RN3



MODIFICATION		
A	12-9-83	
B	30-9-83	
C	25-2-84	
D	15-03-84	182 CMS

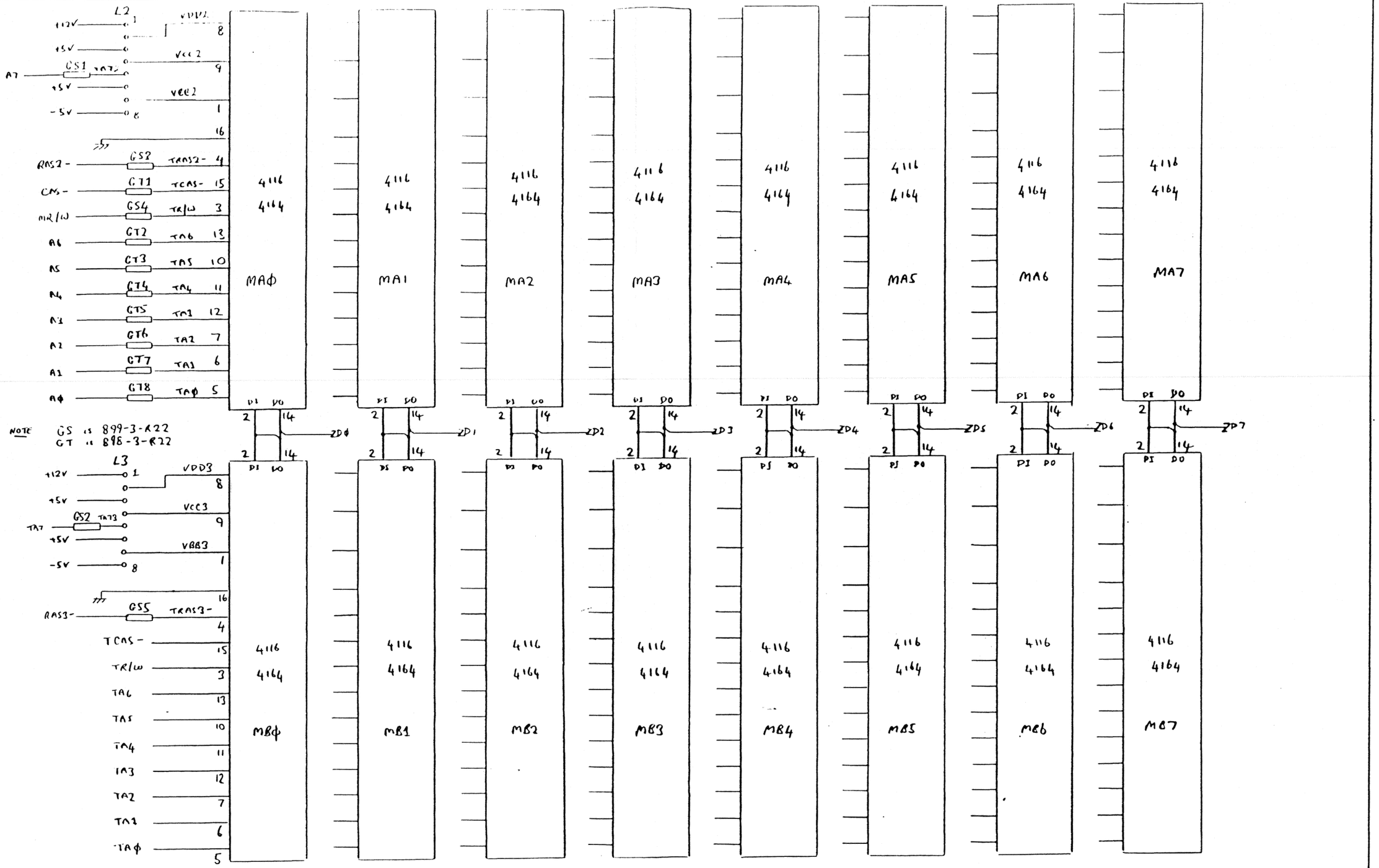
Research Machines Ltd

DATE	DRAWN BY	CHECKED BY
12-9-83	C.A.S.	DSD

TITLE: 480Z MAIN BOARD MK2 TRANSCEIVER

DRAWING NO. D12093. SHT 7 OF 7

WP 1001



NOTE GS is 899-3-R22
GT is 898-3-R22

MODIFICATION			
	Iss	Date	ECN
A	1	29-1-82	
	2	10-Mar-82	

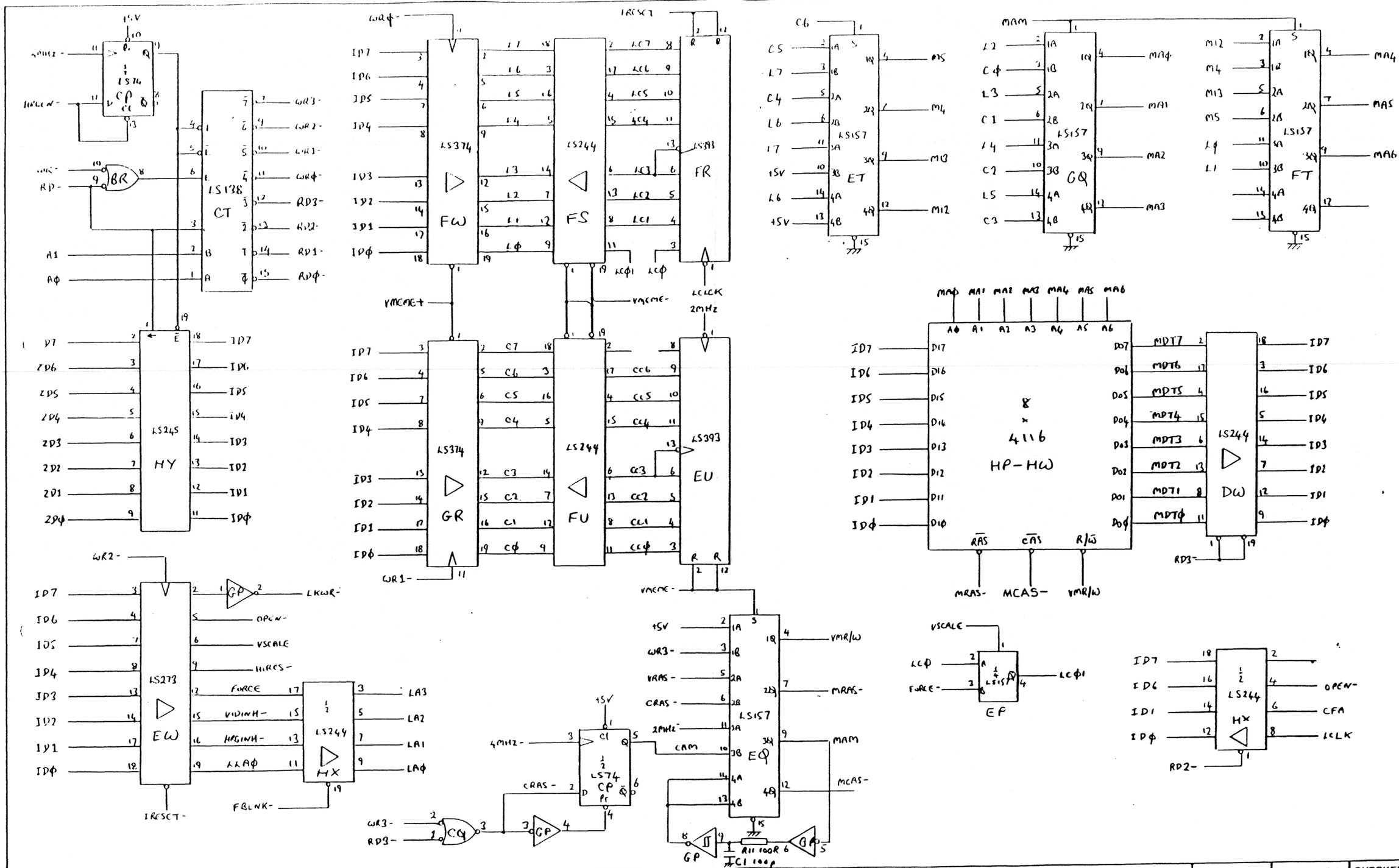
Research Machines Ltd

DATE	DRAWN BY	CHECKED BY
8/12/81	K Ford	

TITLE: LINK 480Z OPTION BOARD - ADD ON RAM.

DRAWING NO. D10830 SHT 1 OF 5

WP 1001



MODIFICATION			
	ECN		
A	Date	29-1-82	10-08-82
Iss	1	2	

WP 1001

Research Machines Ltd

DATE	DRAWN BY	CHECKED BY
8-10-81	K FORD	

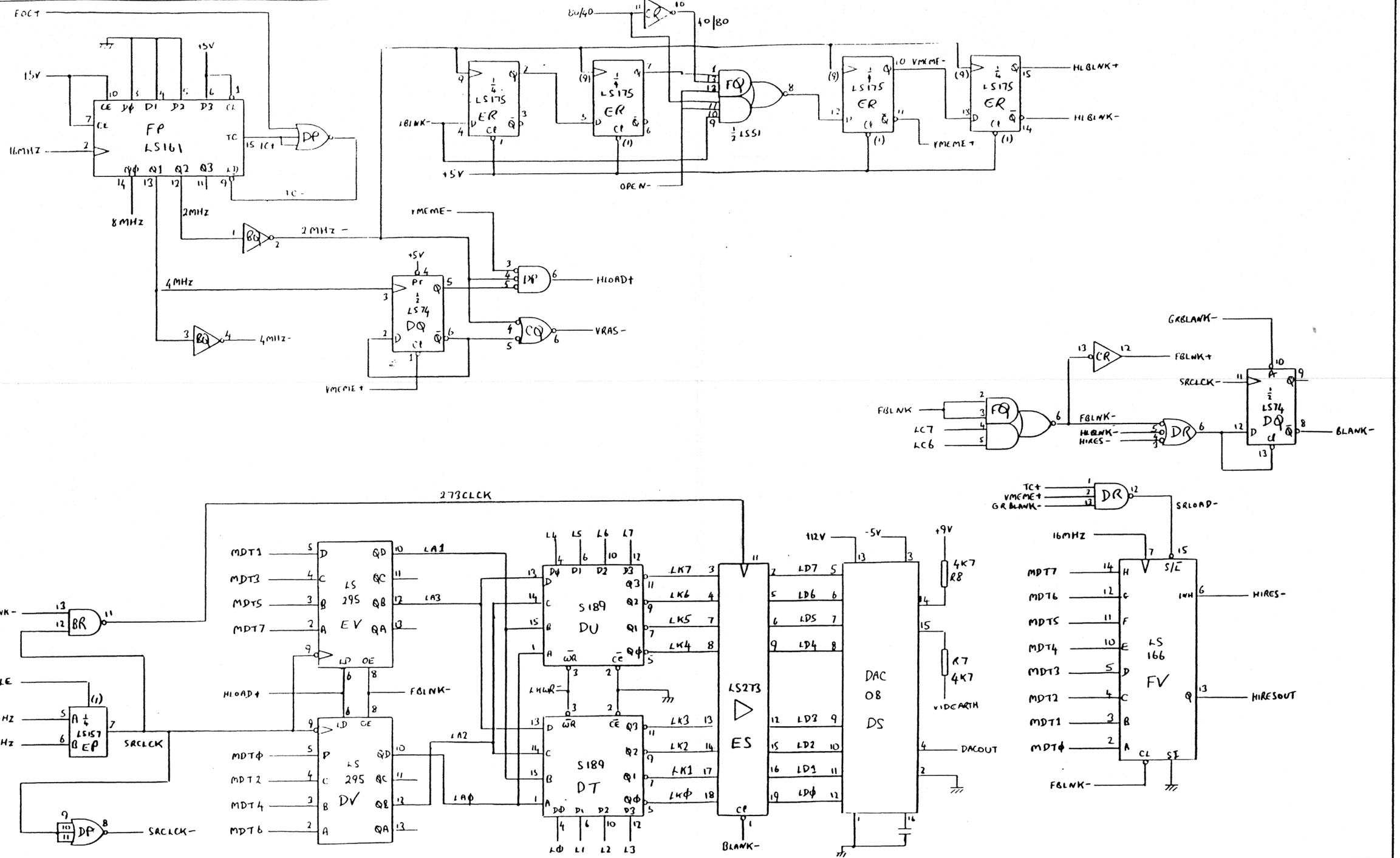
TITLE

LINK 480Z OPTION BOARD

HIGH RESOLUTION GRAPHICS-1, BUS INTERFACE & MEMORY

DRAWING NO.

D10830 SHT 2 OF 5



MODIFICATION		ECN
Iss	Date	
A		
1	29-1-82	
2	10-08-82	

Research Machines Ltd

DATE	DRAWN BY	CHECKED BY
8/10/81	K. Ford	

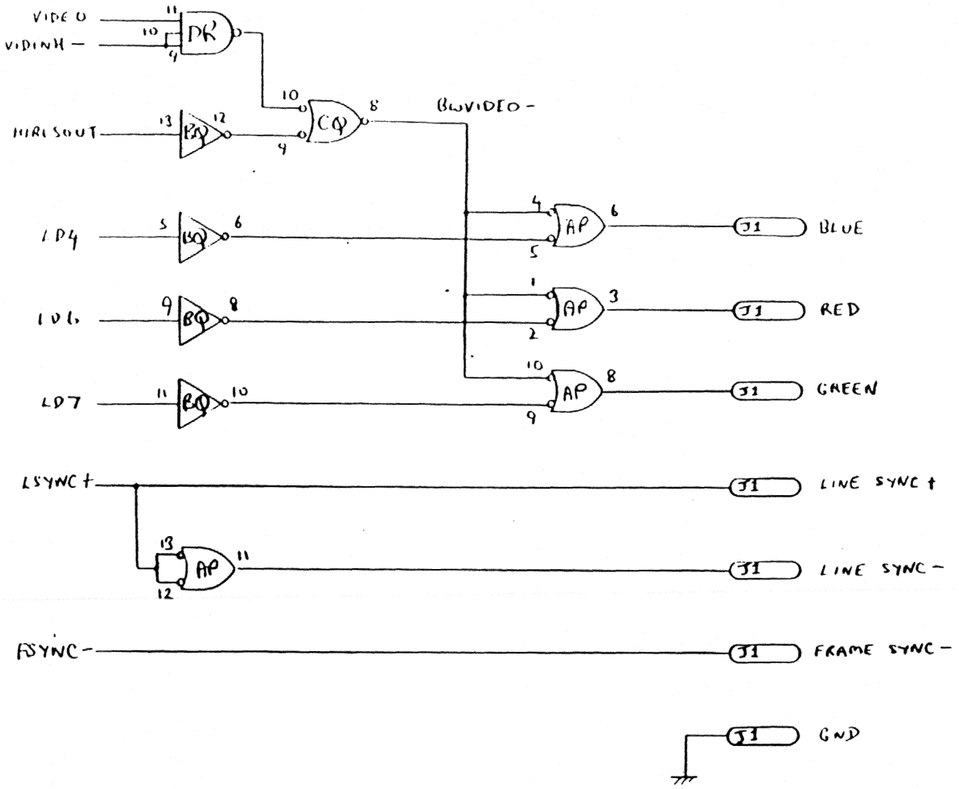
TITLE

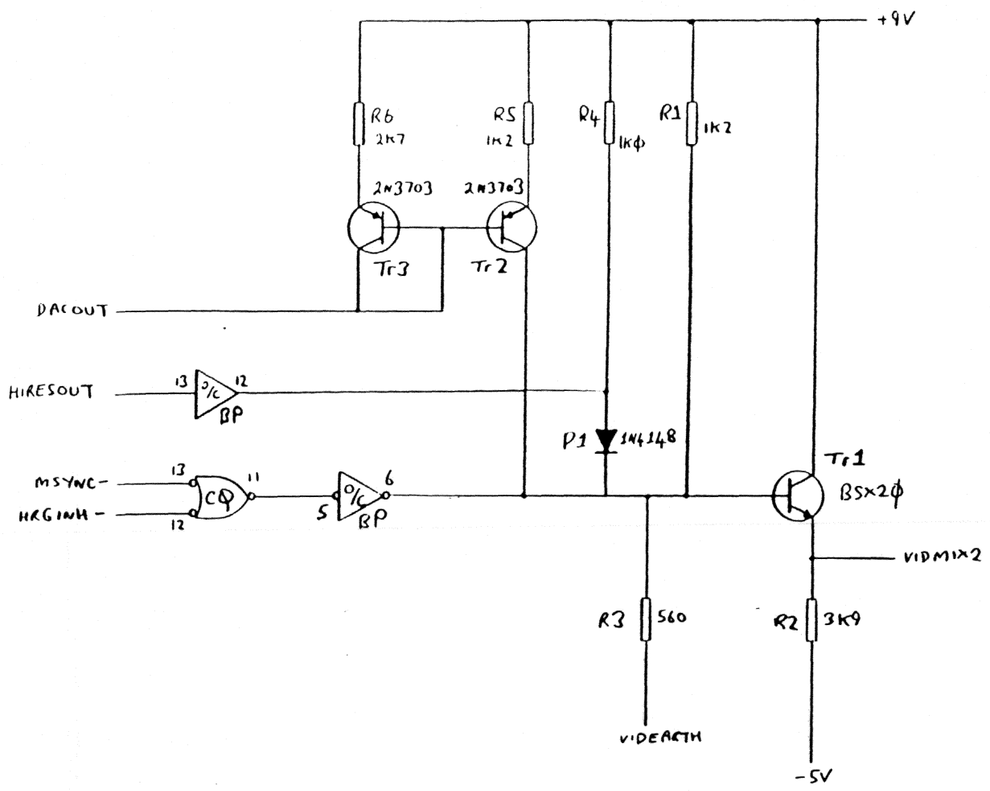
LINK 480Z OPTION BOARD

HIGH RESOLUTION GRAPHICS-2. TIMING & VIDEO GENERATION

DRAWING NO. D10830 SHT 3 OF 5

WP 1001





MODIFICATION	Iss	Date	ECN
A	1	29-1-82	
	2	5-Oct-82	

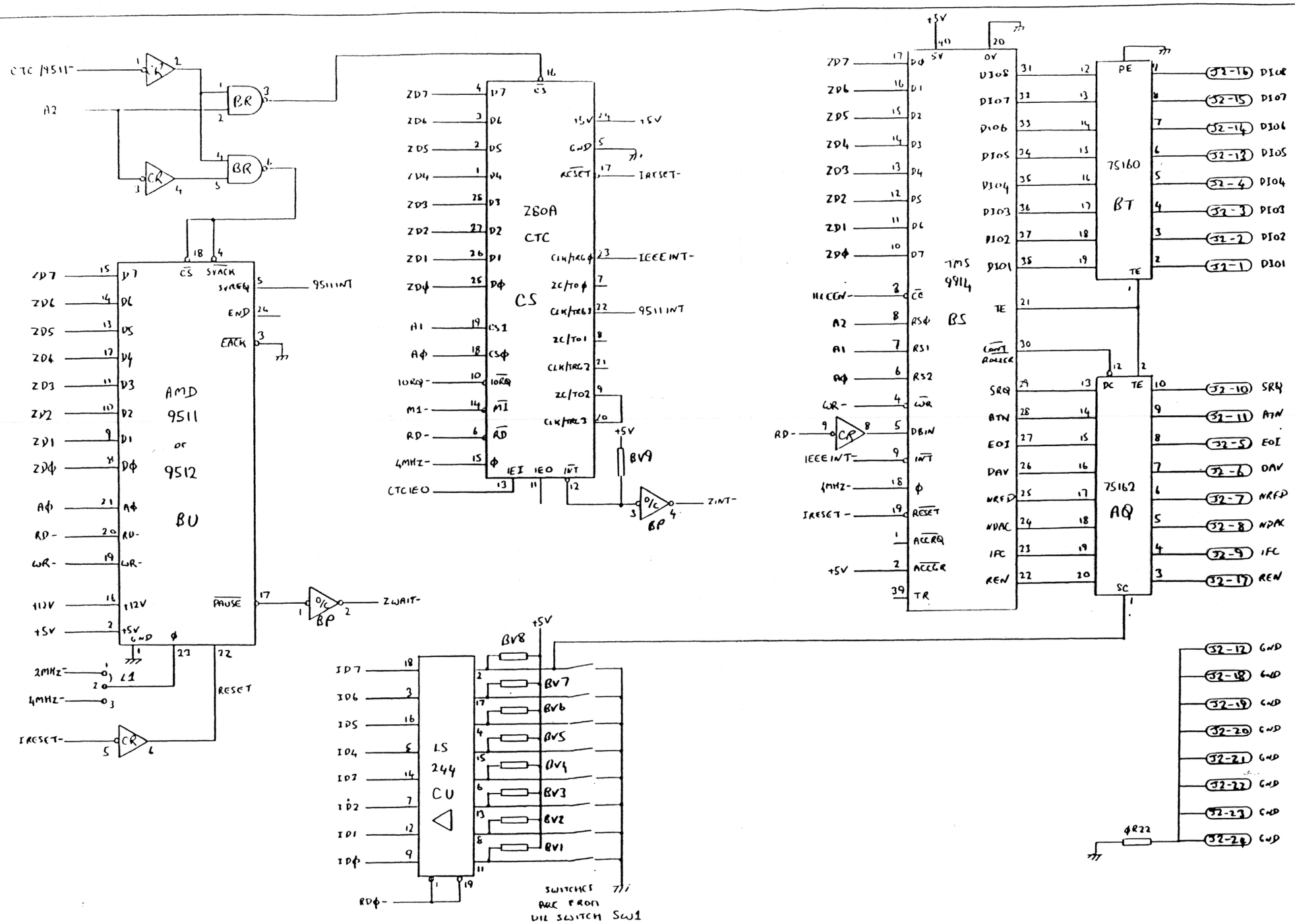
Research Machines Ltd

DATE	DRAWN BY	CHECKED BY
17/12/81	K. Ford	

TITLE: LINK 480Z OPTION BOARD
HIGH RESOLUTION GRAPHICS-3, OUTPUT STAGES.

DRAWING NO. D10830 SHT 4 OF 5

WP 1001



MODIFICATION			
Iss	Date	ECN	
A			
1	29-1-82		
2	10-OCT-82		

Research Machines Ltd

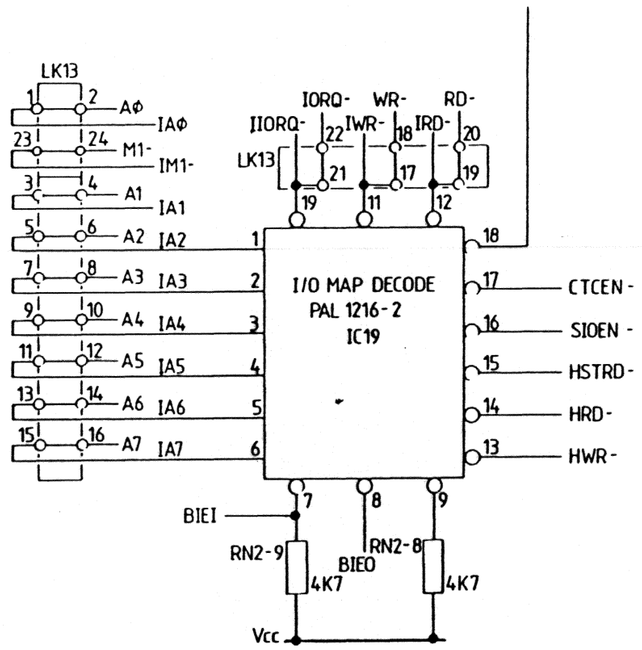
DATE	DRAWN BY	CHECKED BY
16/12/81	K. Ford	

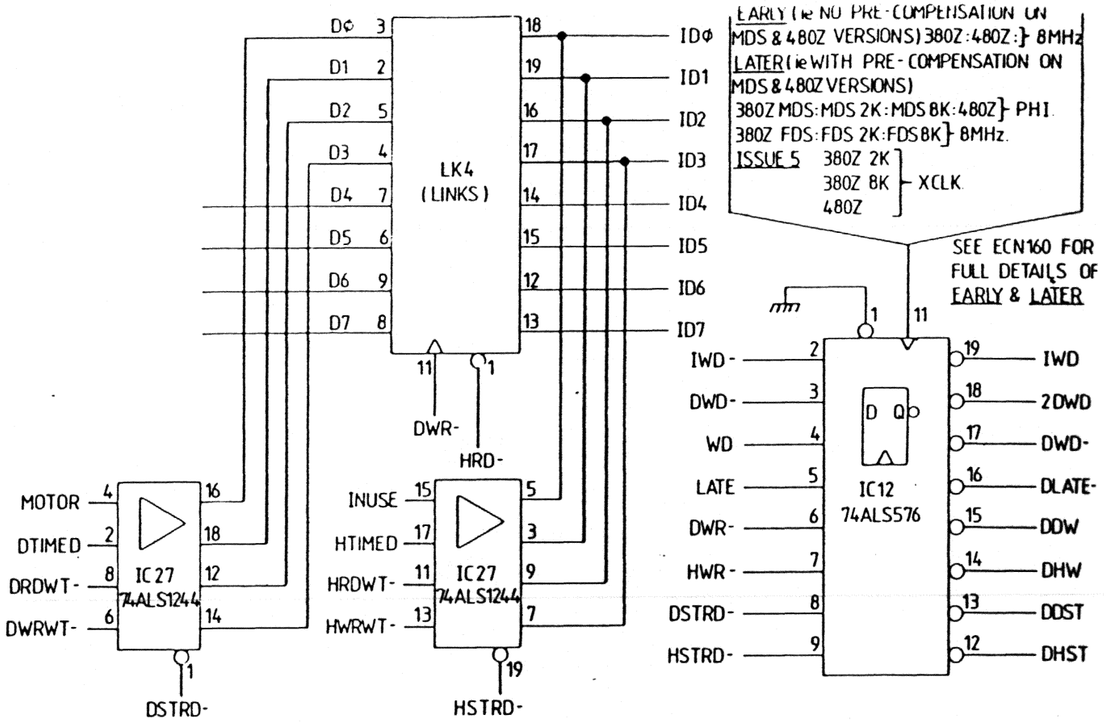
TITLE: LINK 480Z OPTION BOARD
IEEE INTERFACE, MATHS CHIP & CTC.

DRAWING NO. D10830 SHT 5 OF 5

WP1001

DRG. No. D12794 Sht 1 of 4





ECN	Date	Ins.
1	22-2-84	A
108	01-05-84	—

UNLESS OTHERWISE STATED ASSUME
ANGULAR TOLERANCE ± 1 2'
WHOLE UNITS ± 0.5mm
1 DECIMAL PLACE ± 0.1mm
GEOMETRICAL TOLERANCES SEE BS 308 METRIC
THIRD ANGLE PROJECTION

RESEARCH MACHINES

RESEARCH MACHINES LTD, Mill St, Oxford, OX2 0BW

TITLE:
CIRCUIT DIAGRAM IDC 480Z.
(BUS INTERFACE & DECODE)

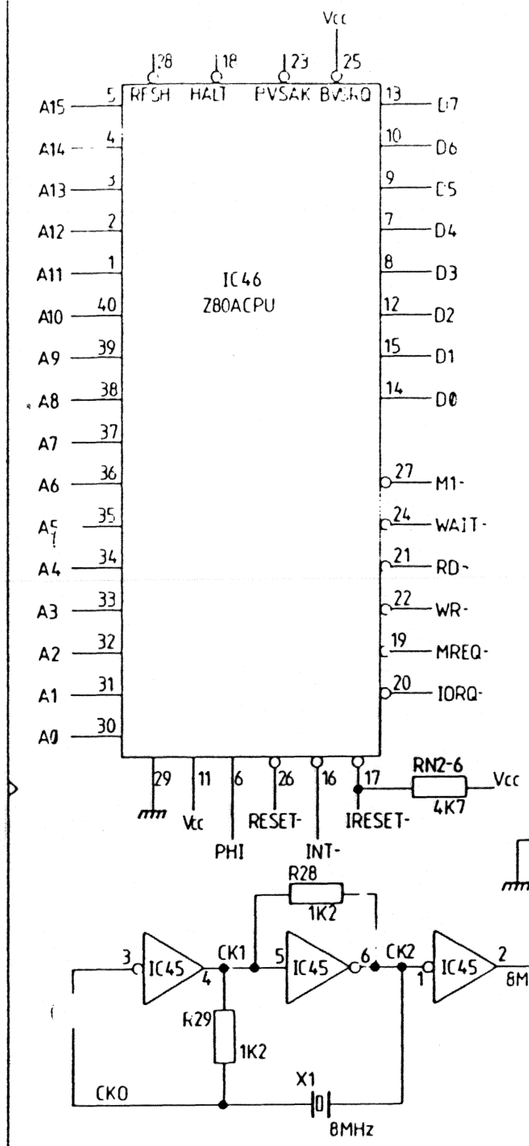
SCALE :

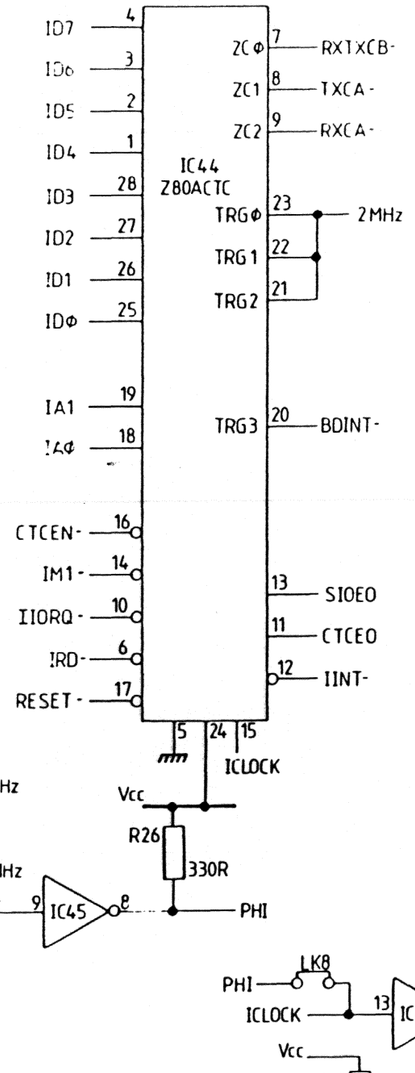
DRN. RB
DATE 22-2-84
APRD. Garth Davis
CHKD. MH

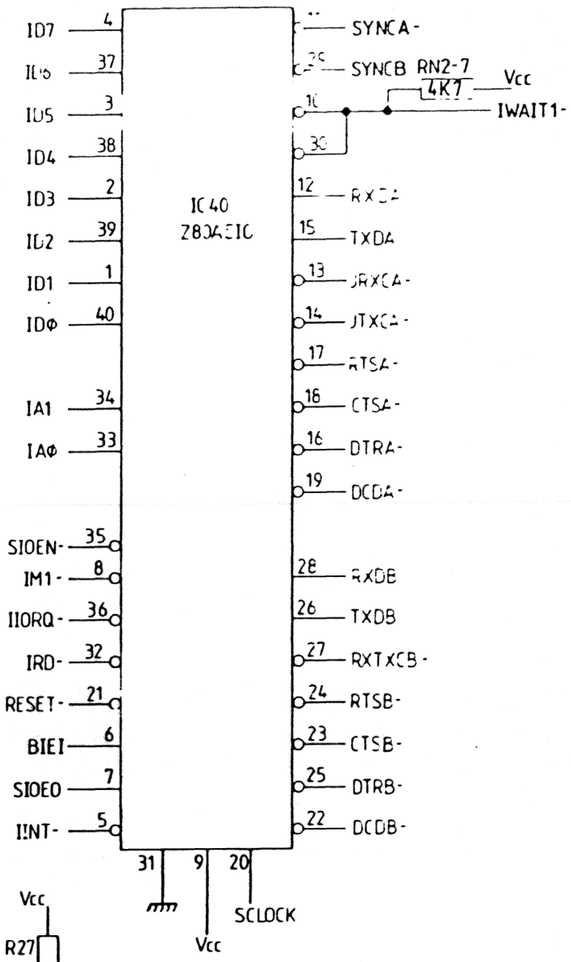
DRG. No. D12794 Sht 1 of 4

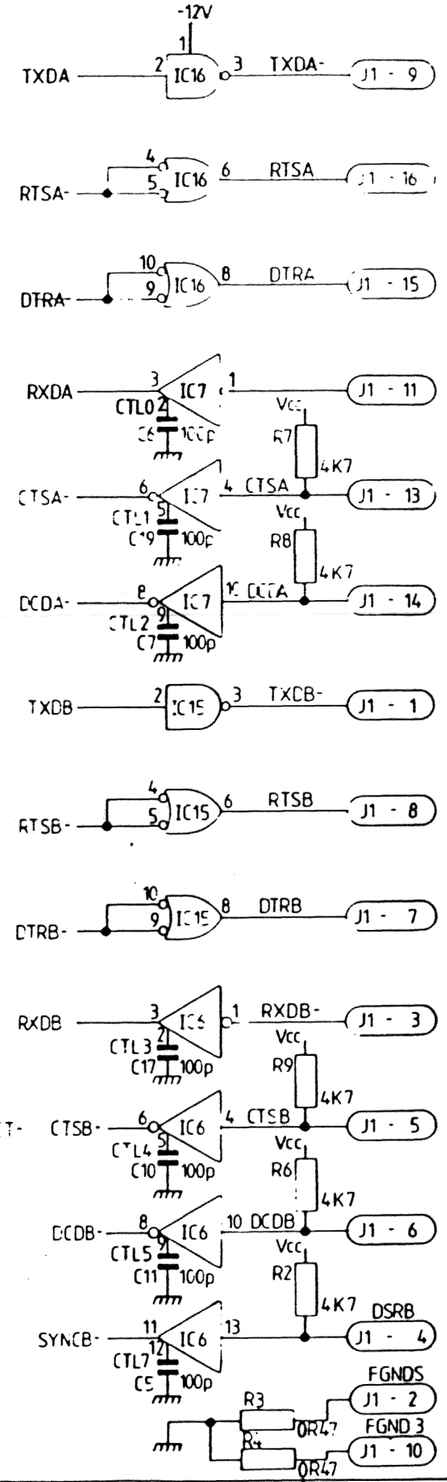
DRG. No. D12794 Sht 2 of 4

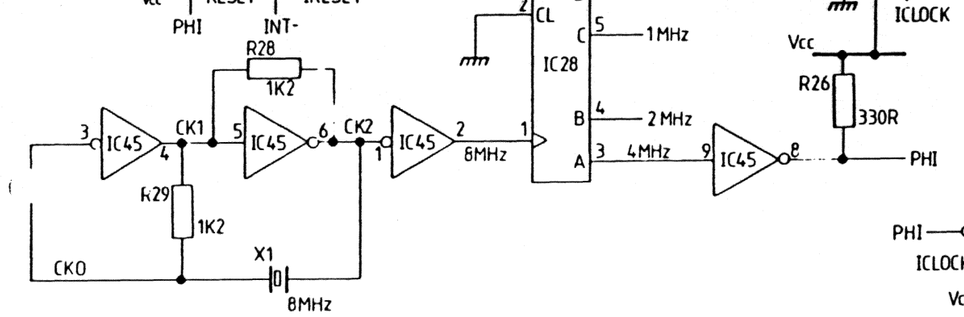
DO NOT SCALE REMOVE ALL BURRS

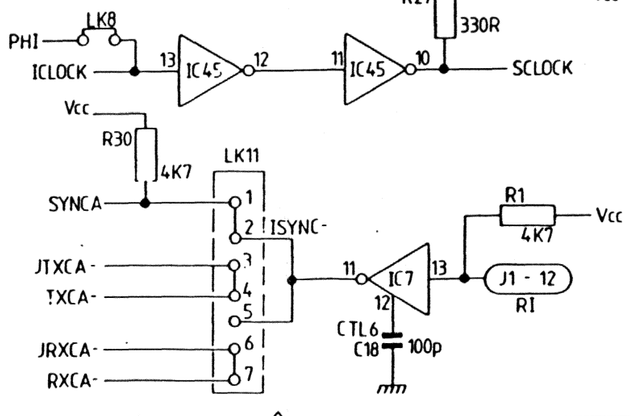


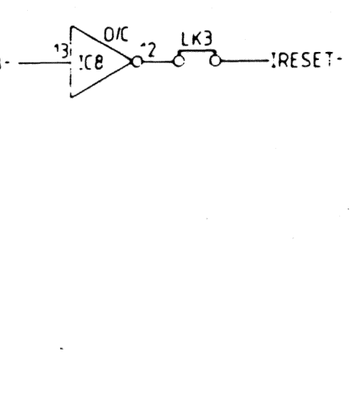












IC No	DEVICE
6 & 7	75189
8	7416
15 & 16	75188
28	74LS393
45	74LS04

E.C.N.	1	208
Date	23-2-84	01-05-84
Iss.	A	1

UNLESS OTHERWISE STATED ASSUME :
ANGULAR TOLERANCE ± 1/2°
WHOLE UNITS ± 0.5mm
1 DECIMAL PLACE ± 0.1mm
GEOMETRICAL TOLERANCES SEE BS308 METRIC
THIRD ANGLE PROJECTION

RESEARCH MACHINES

RESEARCH MACHINES LTD Mill St Oxford OX2 0BW

TITLE : CIRCUIT DIAGRAM IDC 480Z (CPU, SERIAL INTERFACE & CLOCKS)

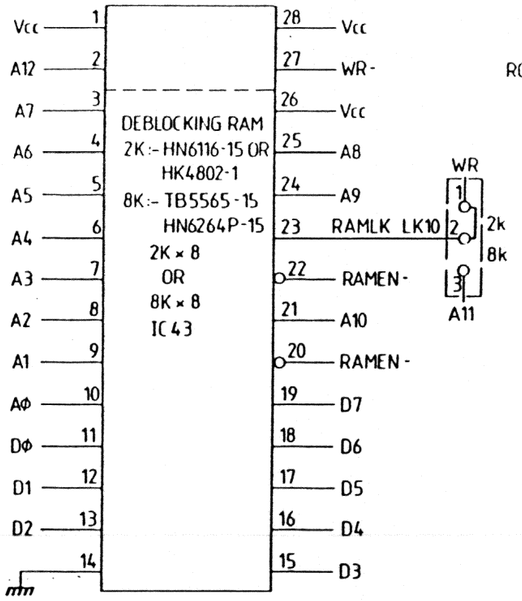
SCALE :

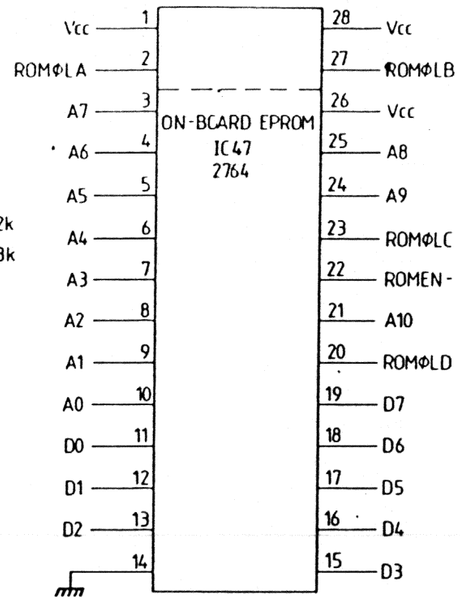
DRN RB | APRD | DATE 22-2-84 | CHKD

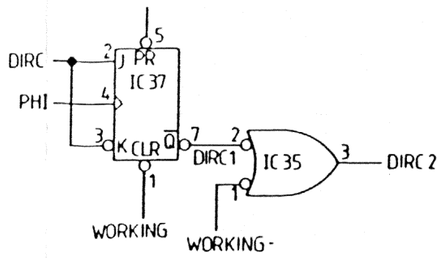
DRG. No. D12794 Sht. 2 of 4.

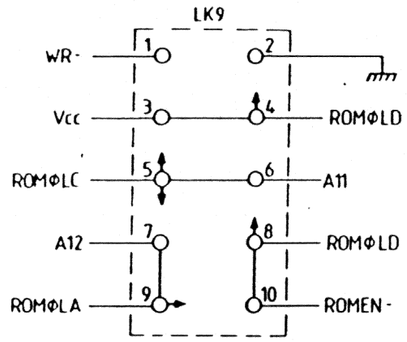
© RESEARCH MACHINES LTD

LK10 LINK PINS 1&2 FOR 2K,
PINS 2&3 FOR 8K



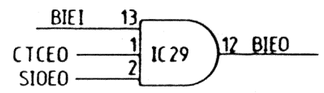


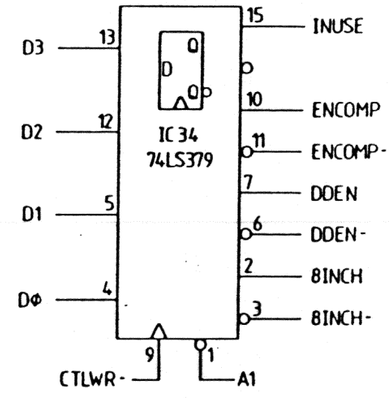


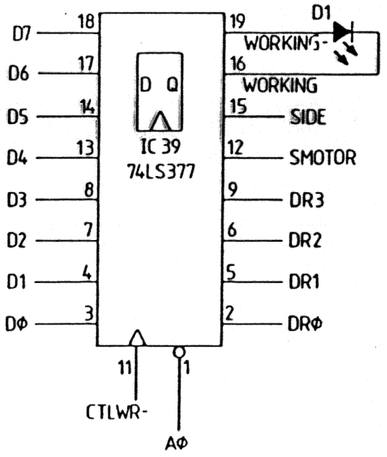


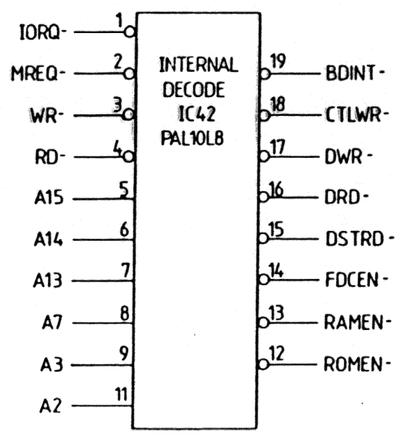
ROM SELECT LINKS LK9
PRE-LINK FOR 2764 OR
LINK FOR DEVICES AS
SHOWN

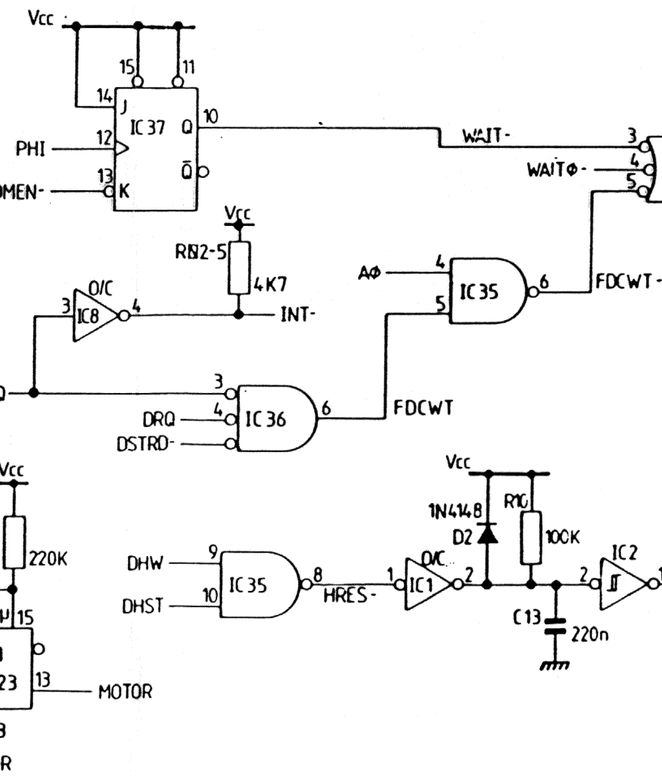
Pin	to	Pin	DEVICE
2	..	4	2564
3	-	5	2516/2532/2716
5	-	6	2732
5	-	7	2564
6	-	8	2532/2564
8	..	10	2716/2516/2732
9		10	2564











IC No.	DEVICE
1	7407
2	74LS244
8	7416
29	74LS11
35	74LS00
36	74LS27
37	74LS109

E.C.N.	Date	
A	23-2-84	1
	01-05-84	208

UNLESS OTHERWISE STATED ASSUME :-
ANGULAR TOLERANCE ± 1/2°
WHOLE UNITS ± 0.5mm
1 DECIMAL PLACE ± 0.1mm
GEOMETRICAL TOLERANCES SEE BS 308 METRIC
THIRD ANGLE PROJECTION

RESEARCH MACHINES

RESEARCH MACHINES LTD. Mill St. Oxford. OX2 0BW

TITLE :
CIRCUIT DIAGRAM IDC 480Z
(MEMORY, WAIT STATE & INTERNAL DECODE)

SCALE :

DRN. RB
DATE 22-2-84
APRD.
CHKD.

DRG. No. D12794 Sht 3 of 4.

1984 RESEARCH MACHINES LTD

DRG. No. D12794 Sht. 4 of 4

IWAIT1 - 13, IWAITΦ - 12 → IC35 → 11 BWAIT

IC3 7416 (O/C)
1 BWAIT → 2 BWAIT
DIRC 2 (3) → 4 DIRN → J2 - 18
HLD (5) → 6 HEADLD → J2 - 2
IWD (9) → 8 WDATA- → J2 - 22
WG (11) → 10 WGATE- → J2 - 24
STP (13) → 12 STEP- → J2 - 20

+12V, Vcc

IC41 FDC MB8877A
D7 14, D6 13, D5 12, D4 11, D3 10, D2 9, D1 8, DΦ 7
RDATA 27, RCLK 26, DDI 37, WG 30, WD 31, VFOE 33, INTRQ 39, EARLY 17, LATE 18, 29
Vcc 40, 21; 1, 20
32 RDY-, 23 Vcc, 6 A1, 5 AΦ, 3 FDCEN-, 4 RD-, 2 WR-, 19 RESET-, 24 FCLK, 34 TRΦ-, 36 WPRT-, 35 IP-, 28 HLD, 16 DIRC, 15 STP, 38, 25 RG, 22 TEST

RN2-4 4K7 → Vcc
R25 4K7
DRQ
C31 100n
IC21 200µs±20% → PDRQ → TP1

RN2-2 4K7 → Vcc
IINT - 3
IC1 7407
DR3 11, DR2 9, DR1 5, DRΦ 13
4 BINT-, 10 DRV3 → J2 - 6, 8 DRV2 → J2 - 14, 6 DRV1 → J2 - 12, 12 DRVΦ → J2 - 10

SIDE 11 → IC8 (O/C) → 10 → J2 - 32 SDSEL-

MOTOR 9 → IC8 (O/C) → 8 → J2 - 16 MOTOR-

RRD - 2 → IC25 25µs±5% (1)
DP8 13 → IC24 16µs±20% (1) → 4 MONO 8 → TP4
Vcc 3, 3
R24 33K, R23 3K9
C37 330p, C25 22n
DRD - 10 → IC25 5µs±5% (9)
DP5 13 → IC24 32µs±20% (9) → 12 MONO5 → TP2
Vcc 11, 11

Vcc
RN1 150R
EREADY1 (J2 - 34) 7
TRKΦ - (J2 - 26) 6
WRTPRT - (J2 - 28) 5
RAWREAD - (J2 - 30) 4
INDEX (J2 - 8) 3
SECTOR (J2 - 4) 2
EREADYΦ (J2 - 6) 8

IC2 74LS244
17, 4, 15, 6, 13, 8, 11; 1, 19
3 READY1, 16 TRΦ-, 5 WPRT-, 14 RDD-, 7 BINDX, 12 BSECT, 9 READYΦ

Vcc
RN2-3 4K7
REV 5 - XRDY
REV 3 - RDY
IC8 (O/C) 1 → 2 → RDY-

LK6
READY1 3
XRDY 2
READYΦ 1

LK6 LINK PINS 1 & 2 WHEN USING 8" DRIVES & BASF 5¼ DRIVES. LINK PINS 2 & 3 IF USING YD 5¼ DRIVES.

LK6 WHEN USING SMC CHIP CUT LINKS 7-8 & 4-5. LINK 8-9 & 4-5.

REV 5 - PHI
REV 3 - XRDY
REV 5 - 8MHz
REV 3 - XRDY

IC31 74LS157
14 4A, 13 4B, 11 3A, 10 3B, 5 2A, 6 2B
12 4Y, 9 3Y, 7 2Y, 4 1Y
REV 5 - XCLK
REV 3 - RDY
IP-
FCLK
MONO
BINDX
BSECT
1MHz
2MHz
SEL STB 1, 15
8INCH

XCK5
LK6
4MHz 6
MONO5 5
8MHz 4
MONO8 7
XCK8
2, 9, 8, 3 → 1A, 1B

J2 - 1, J2 - 3, J2 - 5, J2 - 7, J2 - 9, J2 - 11, J2 - 13, J2 - 15, J2 - 17, J2 - 19, J2 - 21, J2 - 23, J2 - 25, J2 - 27, J2 - 29, J2 - 31, J2 - 33

R5 0R47

Vcc
RN2-10 4K7
C45 100n
8INCH -
PDRQ
RDD -
DDEN
MONO

VFO DIGITAL MODULE 1 IC26 MB14323
16, 8; 10, 11, 2, 3
15 PR-1, 14 UP, 12 DOWN, 13 CP1 → TP3, HG
9 MB, 7 MA, 6 SB, 5 CP2, 4 RCLK → TP5

VFO DIGITAL MODULE 2 IC33 MB14324
15, 14, 5, 7; 16, 8
3 FR, 4 SPD, 2 SPC

IC36 (13, 1, 2) → 12 LK4 → RDATA → TP7

WHEN USING SMC CHIP REMOVE IC17,23,24,25,26, 32&33 & CUT LINK LK4.

R13 10K → FS 11
R14 560R PA0, C38 22n
R15 3K9 PL0, C29 4n7
R17 18K HI0
R16 510R AI 12
LO 13, AO 10, VCO 9
R18 820R
VFO ANALOG MODULE IC17 MB4393.
15 UP, 14 DOWN, 12 CP1 → TP3, 13 HG, 3
4, 7 VC1, C28 100n, 6 VCΦ 16, 8
Vcc

IC32 SMC 9216B
MONO 3, RDD - 1, DDEN - 5, 6 CDΦ, CD1 4
2 RCLK, 7 RDATA

IC N°	DEVICES
8	7416
21,24,25	74LS123
36	74LS27

E.C.N.		
Date	23-2-84	01-05-84
	A	—

UNLESS OTHERWISE STATED ASSUME :-
ANGULAR TOLERANCE ± 1/2°
WHOLE UNITS ± 0.5mm
1 DECIMAL PLACE ± 0.1mm
GEOMETRICAL TOLERANCES SEE BS308 METRIC
THIRD ANGLE PROJECTION

RESEARCH MACHINES
RESEARCH MACHINES LTD, Mill St, Oxford, OX2 0BW.

TITLE :
CIRCUIT DIAGRAM IDC 480Z
(DISK DRIVE INTERFACE)

SCALE :

DRN. RB | APRD. | DATE 22-2-84 | CHKD.

DRG. No. D12794 Sht. 4 of 4

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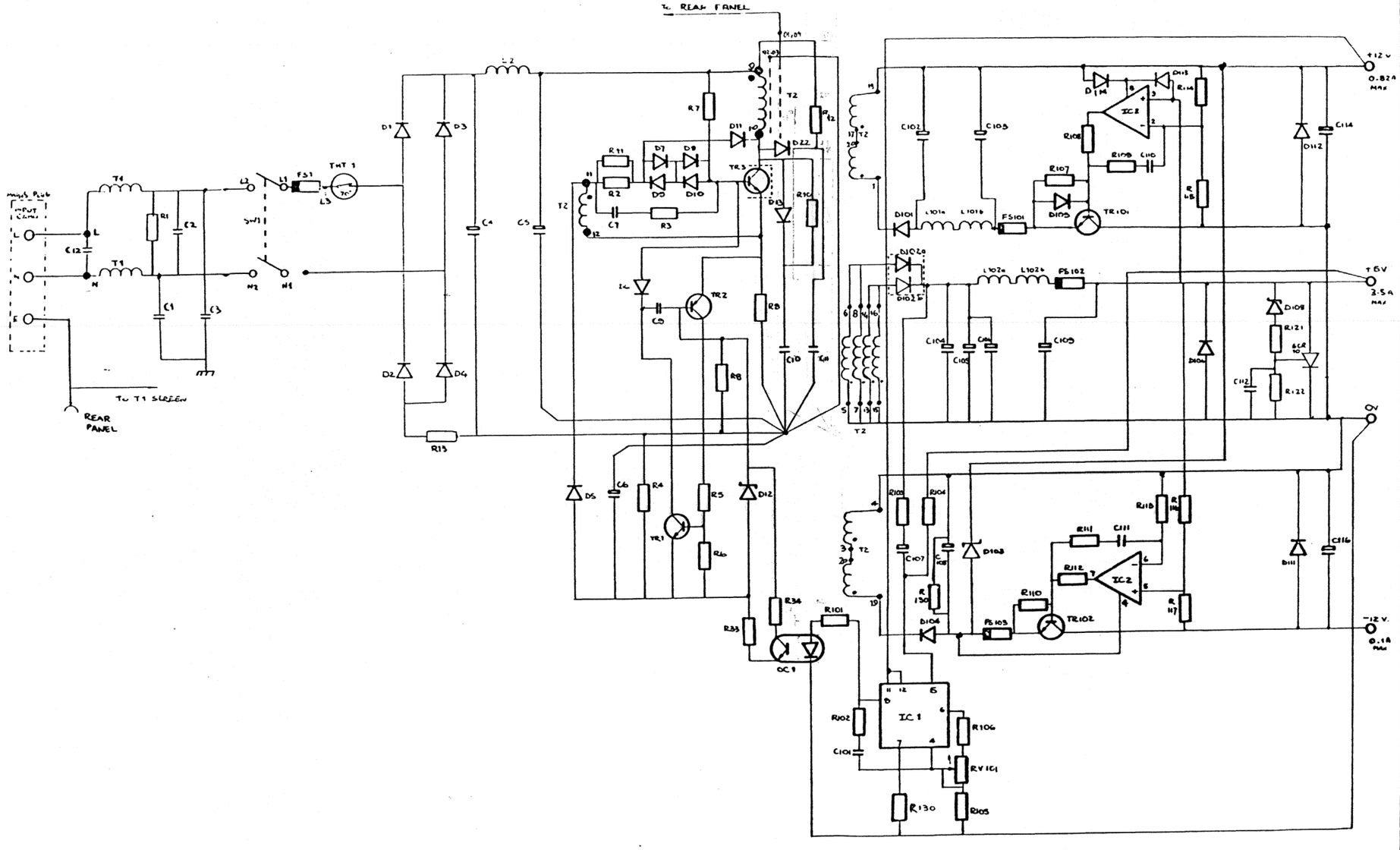

N.B. C107, C111, R108, R111 — NOT FITTED

DRG OR PART NUMBER	DESCRIPTION		
R1	RESISTOR 1MΩ 1/4W		1
R2, R11	" 100Ω "		2
R3	" 47Ω 1/4W		1
R4 R104	" 4K7 "		1
R5, R6, R103, R113	" 1K "		
R8 R105	" 10Ω "		2
R7	" 3M3Ω 1/4W		1
R9	" 0.39Ω 3W		1
R10	220Ω 6W RESISTOR		1
R12	RESISTOR 33Ω 2W		1
R13	" 10Ω 5W		1
R101	" 180Ω 1/4W		1
R102	" 18K "		1
R103	" 15K 1/4W		1
R107	" 39Ω 1/4W		1
R114	" 1K4 0.5% 2W		1
R115, R116	" 1K " "		2
R117	" 2K4 " "		1
R118	" 390Ω 1/4W		1
R121	" 100Ω 1/4W		1
R33, R34	" 4.7Ω 2W 5%		2
D113, D114	DIODE F.R.C. FR 151		2
D1, D7, D8, D9, D10 D106	" 1N4004		6
D11, D13 D22	" RGP 15 B		3
D12	" ZENER C22V		1
D101, D111, D112	" IN5404		3
D102	" BYX55/400		1
D1, D2, D3, D4 D105	" IN5061 *		4
D5, D104	" RGP 15 B		2
D103	" ZENER 33V 5%		1
D 108	" ZENER 5%		1
C1, C3, C11	CAPACITOR 330nF 275V A.C.		3
C2, C12	" 0.1μF 275V A.C.		2
C4, C5	" 33mF 35V		2
C6	" 150μF 25V		1
C7	" 4700pF 50V		1
C116	" 47mF 25V		1
C9	" 22000pF 50V		1
C112, C110	" 0.01μ 250V		2
C108 C105 C106 C109	" 2200pF 16V		4
C101	" 0.047μF 63V		1
C102	" 330μF 63V		1
C10	" 470μF 10V		1
C108	" 220μF 10V		1
R109	RESISTOR 560Ω 1/2W		1
R122	" 220Ω "		1
FS1	FUSE 1A S-20		1
FS101	" 1.25A S-20 F		1
FS102	" 4A S-20 F		1
FS103	" 0.2A S-20 F		1
THT 1	THERMAL CUTOUT 70°C		1
R130	RESISTOR 470Ω 1/2W		1
TR1	TRANSISTOR BC 182		1
TR2	" BC 212		1
TR3	" BU 426A		1
TR101	" 2N3055		1
TR102	" BD131		1
OC1	O.C. H11A2		1
SCR 101	THYRISTOR MCR 106-1		1
IC1	I.C. MC 1723L		1
IC2	" MLM 368L		1
R10	RESISTOR 1K 6W		1
C114	CAPACITOR 820μF 25V		1
C103	RESISTOR 150Ω 6W		1

CHANGE	ISSUE	DATE	CHANGE	ISSUE	DATE
	A1624 G	2			
	A1620M	1			16/7/81
		A			18-2-81

DRAWN	APP	TOL	ALL DIMENSIONS IN m.m.

SCALE

GRESHAM LION LTD. (ASHINGTON DIVISION)

TITLE
CIRCUIT DIAGRAM — RESEARCH MACHINES P.S.U.

SHT 1 OF 1

DRG OR PART NO
320470/1/030

POWER PINS:

		0v	+5v
IC1	4051	6,7,8	16
IC2	3046	13	1,?
IC3	4013	7	14
IC4	4031	8	16
IC5	4070	7	14
IC6	4081	7	14
IC7	4028	8	16
IC8	4040	8	16

IC2
3046 TRANSISTOR ARRAY

--	A			MATERIAL	DIMS IN mm/ INCHES	alphameric Alphameric Keyboards Limited Manor Way Old Woking Surrey GU 22 9JX	
					SCALE	TITLE RESEARCH MC's 65 key	Customer
					FINISH		DRAWING NUMBER 144 - 1710 SHT